

# Compal Confidential

## NIMUA/UB

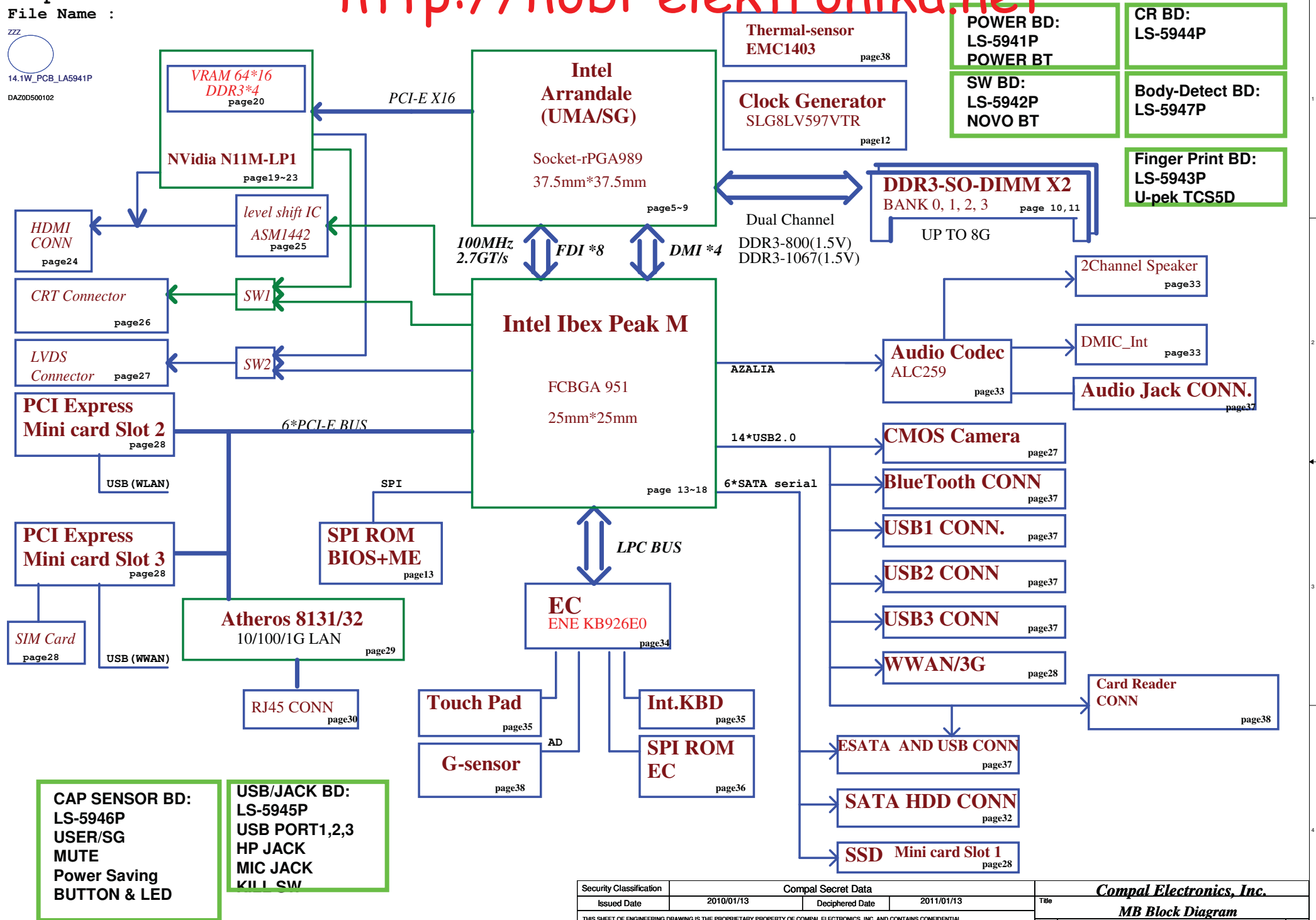
### Schematics Document

### Arrandale

with Intel IBEX PEAK-M core logic

REV : 0 . 3

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Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>MB Block Diagram</b>	
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# DDR3 Voltage Rails

power plane				+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS For SG +3VS_DELAY +1.8VS_VGA +1.5VS_VGA
State	+B	+5VALW +3VALW	+1.5V	
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

## @ FUNCTION

PVT	NON-USE
45@ (45 BOM)	
100@ 10/100 LAN	
GIGA@ GIGA LAN	
UMA HDMI@ FOR UMA HDMI components	
HDMI@ FOR HDMI components	
3G@ 3G(WWAN) function	
X76@ (X76 BOM)	
ESATA@ ESATA function	
CMOS@ Camera function	
SSD@ SSD w/ miniPCIE socket	
10M@ FOR 10M CHIP	
11M@ FOR 11M CHIP	
UMA@ UMA only (Arranddale)	
DIS@ DIS only (Arranddale)	
VGA@ FOR NVIDIA PART	
HYBRID@ FOR SWITCHABLE	
HU@ SWITCHABLE or UMA only	
HD@ SWITCHABLE or DIS only	

## SKU

Arrandale(dGPU) <del>DIS only</del>	DIS@ / 100@ for EVT
Arrandale(iGPU) UMA only	UMA@ / 100@ for EVT
Arrandale(iGPU+dGPU) SWITCHABLE	HYBRID@

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## SMBUS Control Table

	SOURCE	RAM M2	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	N11x Thermal Sensor	EMC1403	Cap sensor board	ALS	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	V	X	X	X	V	V	X	V	V
SMB_EC_DA2	+3VALW			+3VALW				+3VS	+3VS		+3VS	+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	X	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS						
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	X	X	X	X	X
SML1DATA	+3VALW											

## PCH, I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

## EC, I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
PCH	96/98,R/W	1001011X 1001100X
EMC1403 Thermal sensor	9A	1001101X
N-vidia Thermal sensor	9E	1001111X
ALS	70/72,R/W	0111000X 0111001X

## PCIE PORT LIST

PORT	DEVICE
1	<del>NEW CARD</del>
2	WLAN
3	LAN
4	3G
5	
6	
7	
8	

## SATA PORT LIST

PORT	DEVICE
0	HDD
1	SSD
2,3	HM55 disabled
4	E-SATA
5	

## USB PORT LIST

PORT	DEVICE
0	USB 1
1	USB/ESATA
2	CMOS
3	USB 2
4	
5	CARD READER
6	X HM55 disabled
7	X HM55 disabled
8	WIRELESS
9	USB 3
10	FingerPrinter
11	BT
12	
13	3G

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VGA and DDR3 Voltage Rails (N11M GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	HDMI_DETECT_VGA
GPIO2	OUT	H	NV_INVTPWM
GPIO3	OUT	H	VGA_ENVDD_R
GPIO4	OUT	H	VGA_ENABLT
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	
GPIO8	I/O	L	
GPIO9	OUT	L	
GPIO10	OUT		
GPIO11	I/O	L	
GPIO12	IN	-	
GPIO13	OUT	-	
GPIO14	OUT	-	
GPIO15	IN	-	
GPIO16	OUT	-	
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	
GPIO20	IN	-	
GPIO21	IN	-	
GPIO22	IN	-	
GPIO23	I/O		

	Device ID
N11M-LP1 (40nm)	0x0A6E

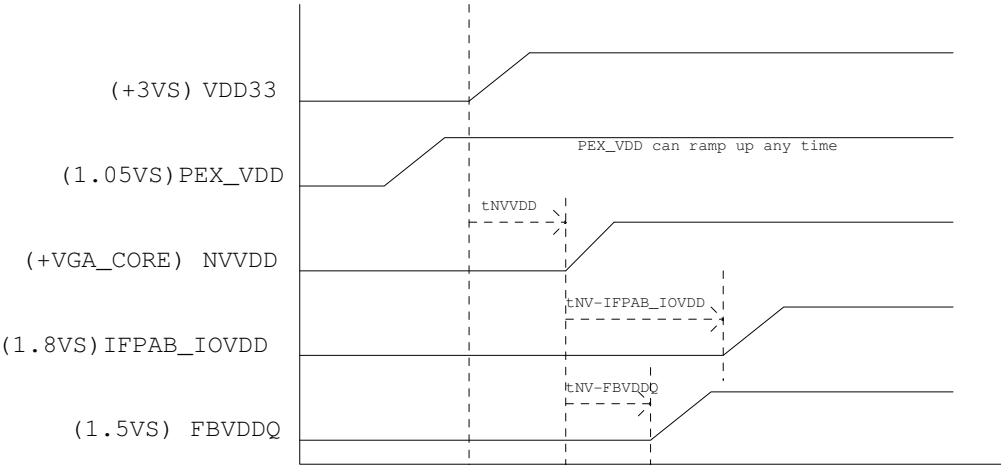
GPIO5 GPIO6

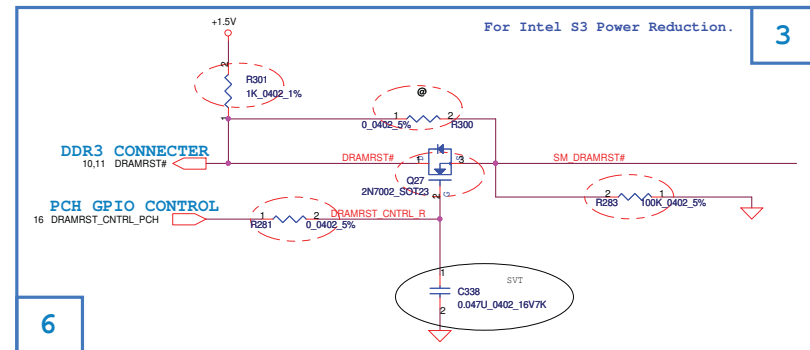
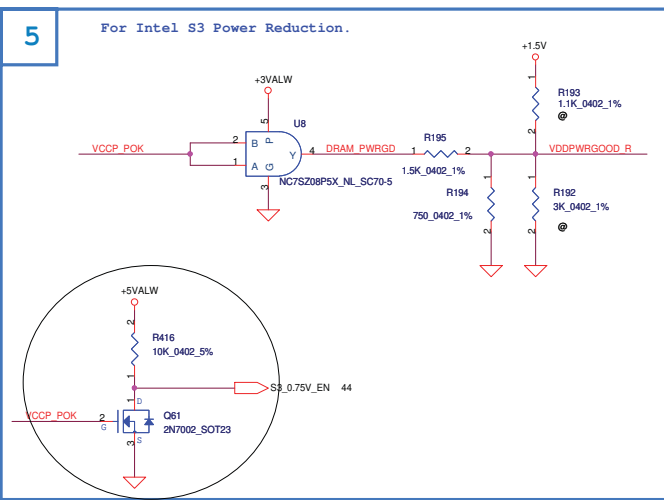
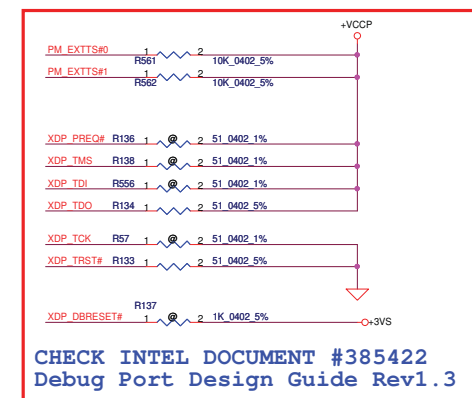
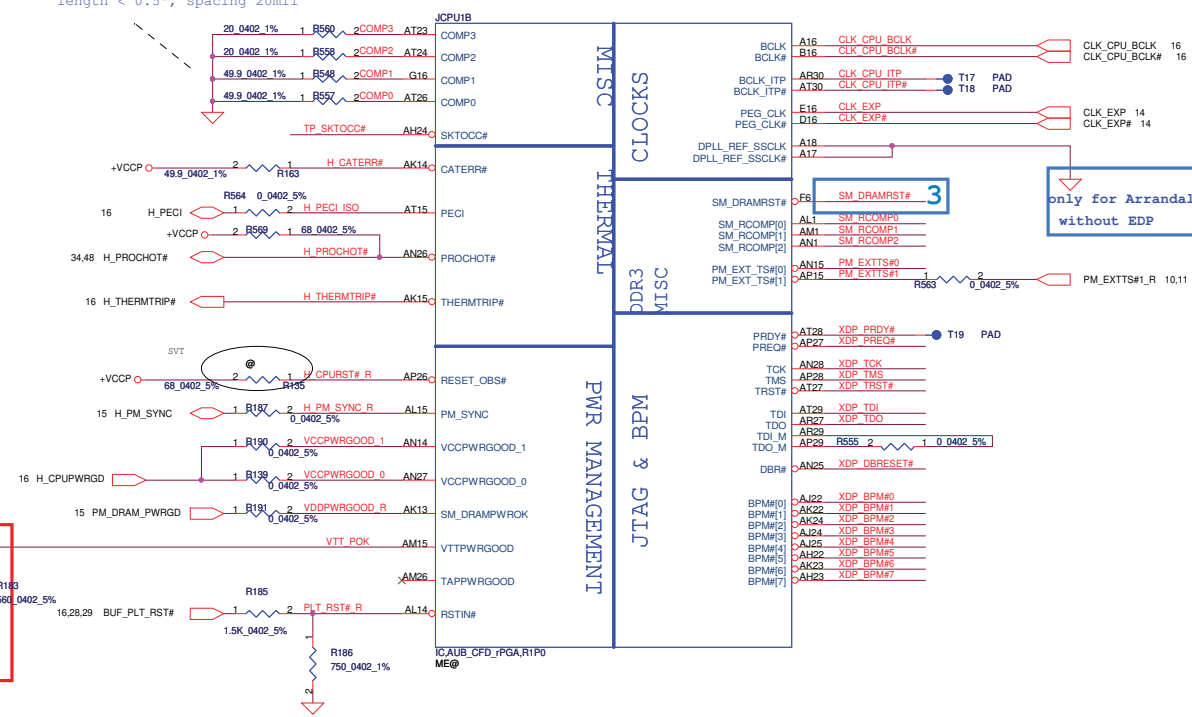
GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.86V	P0

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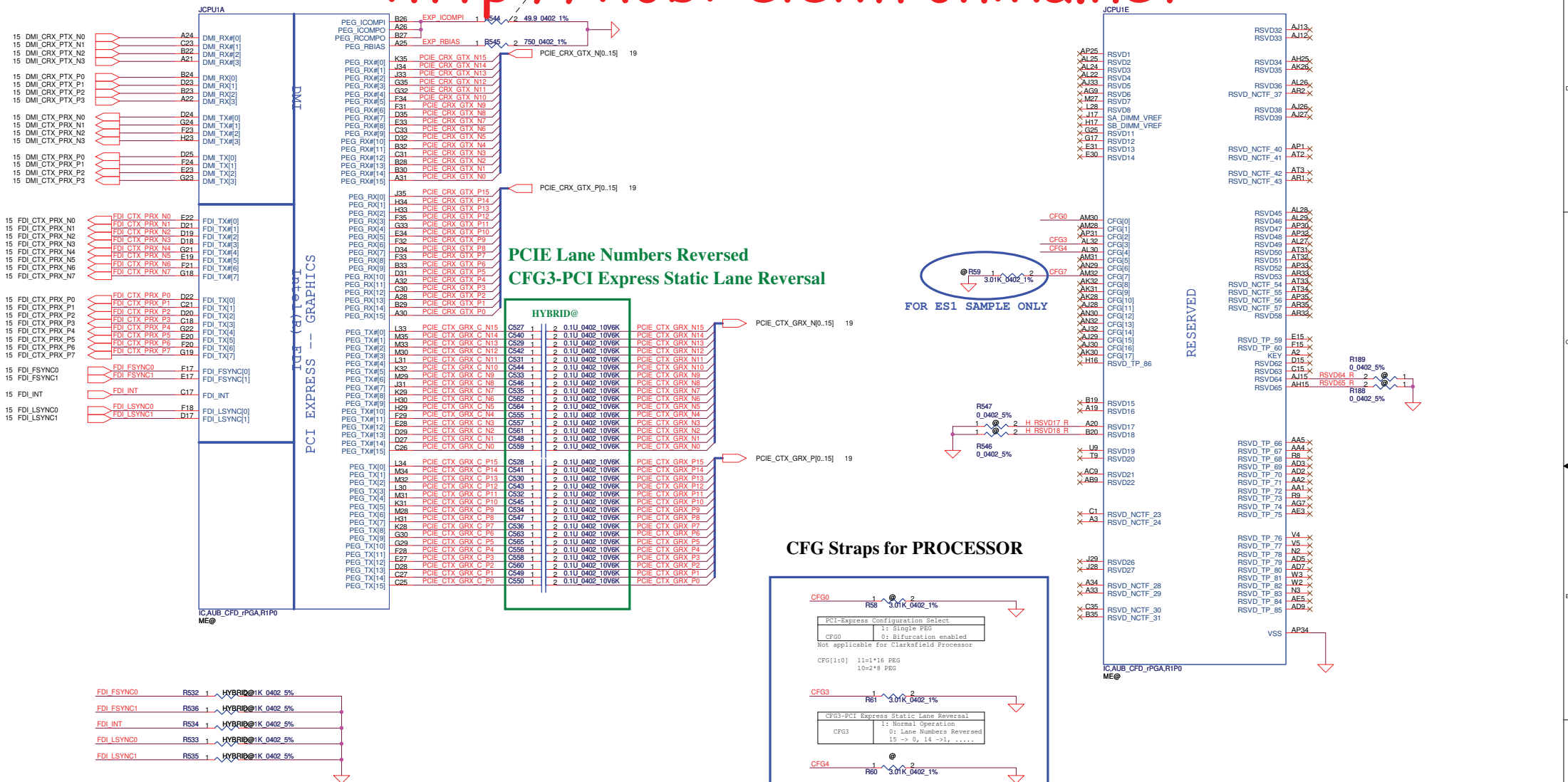
Power Sequence

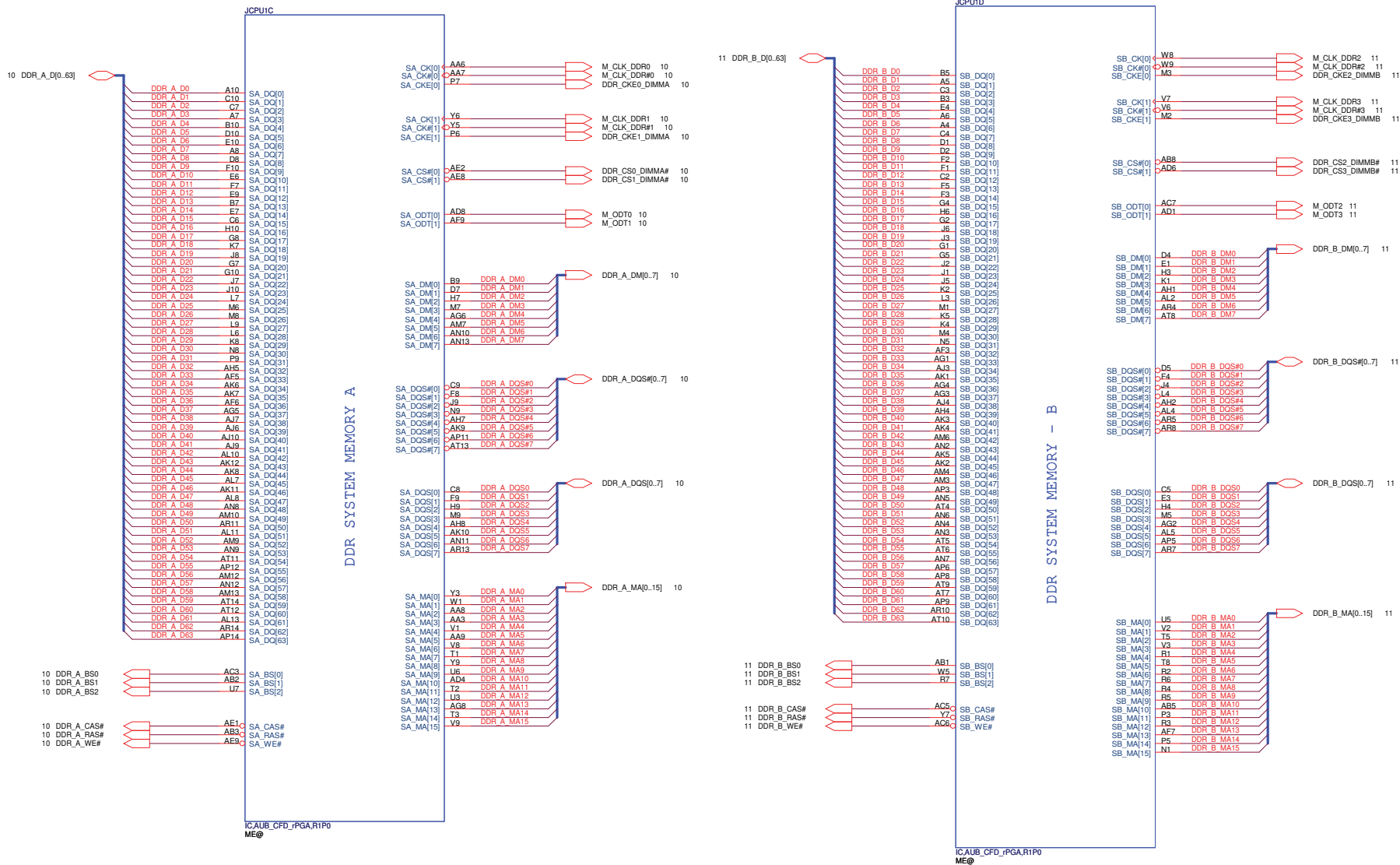
The ramp time for any rail must be more than 40us





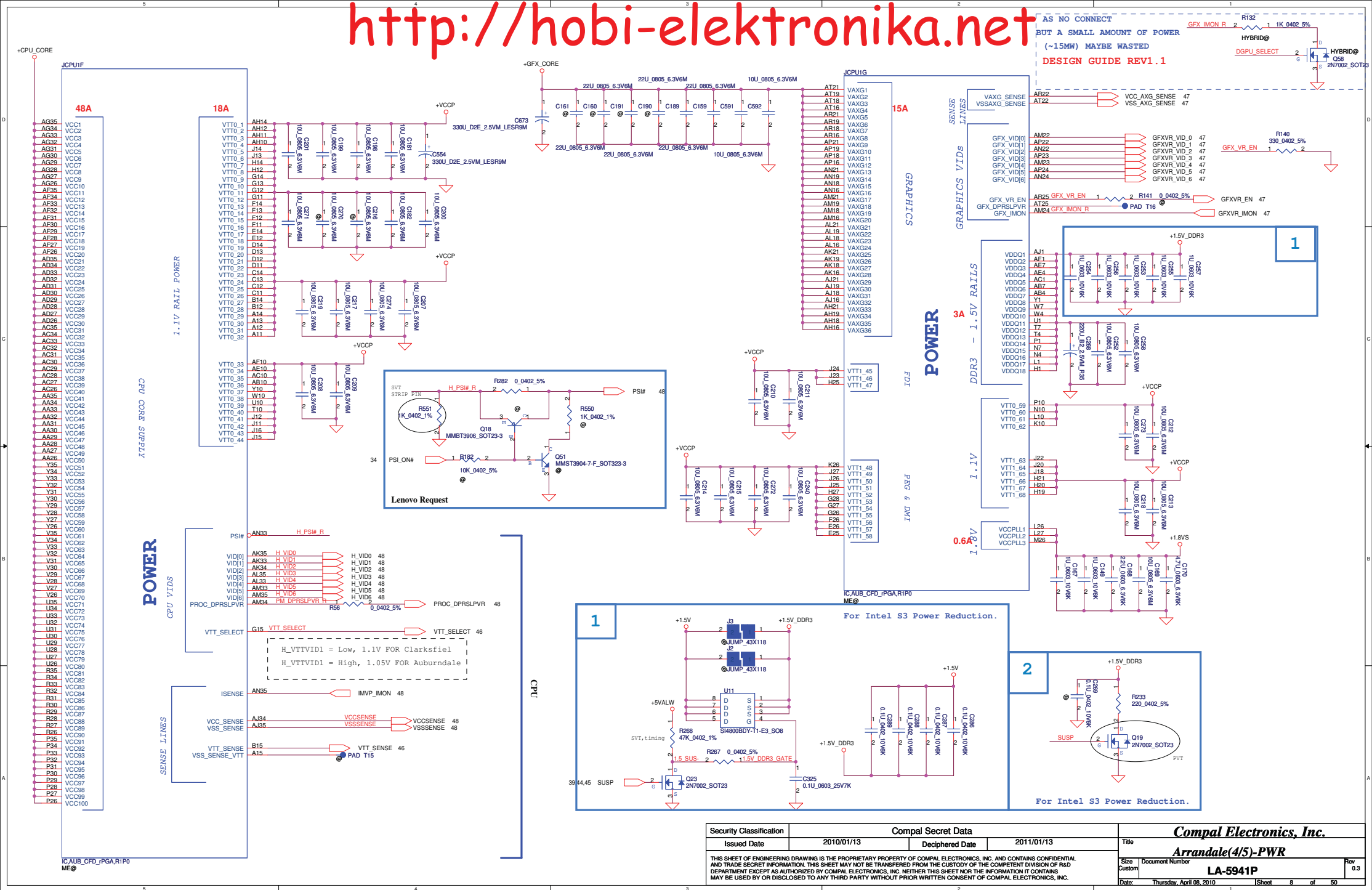
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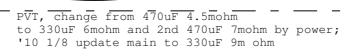


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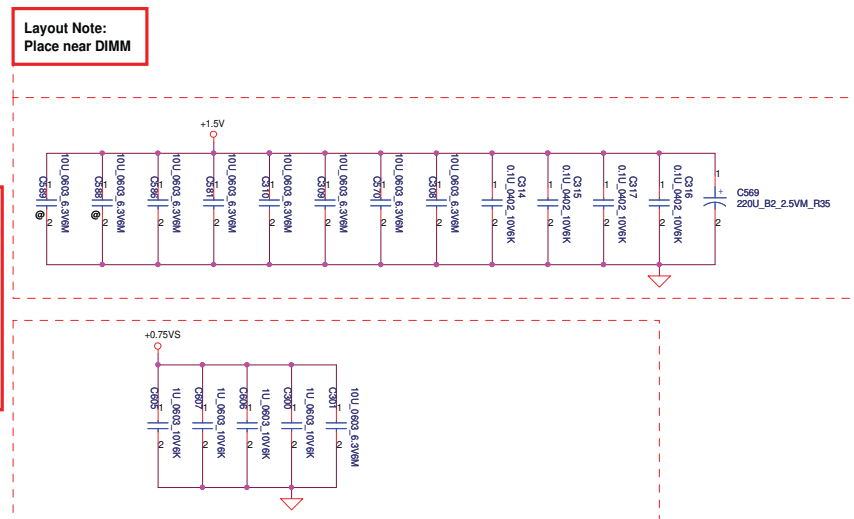








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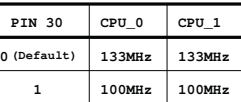


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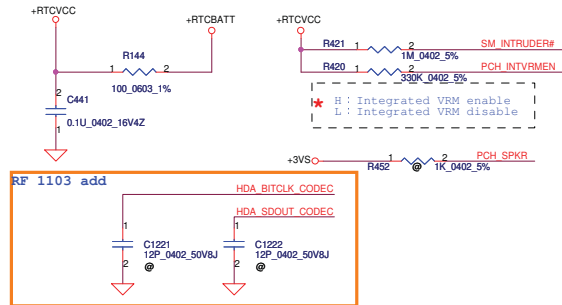
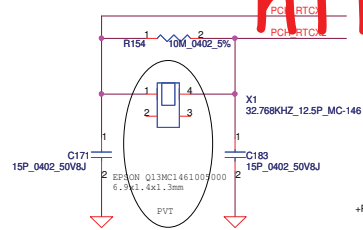




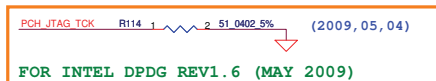
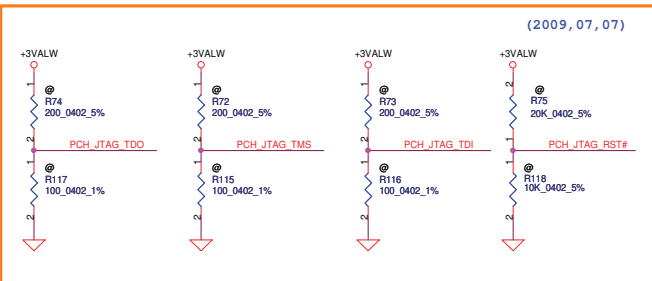
- 1. 27M\_CLK
- 1. 27M\_CLK\_SS



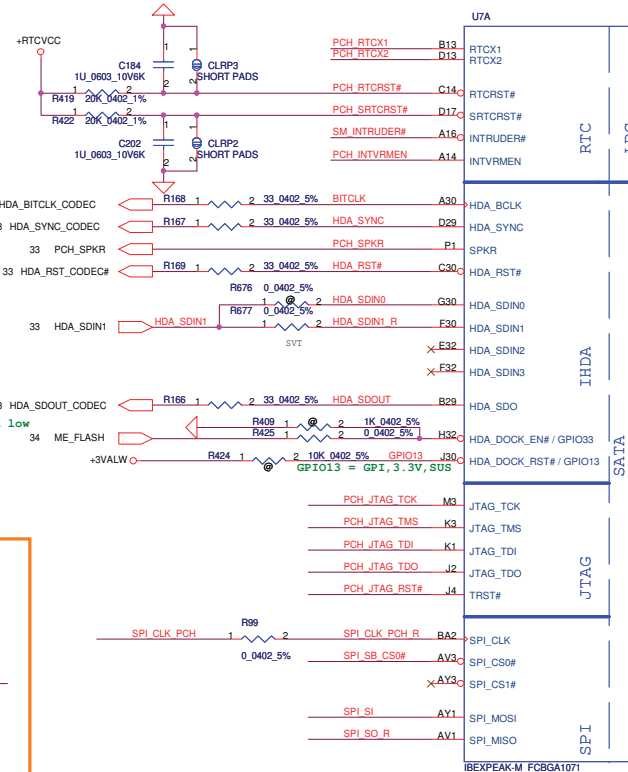
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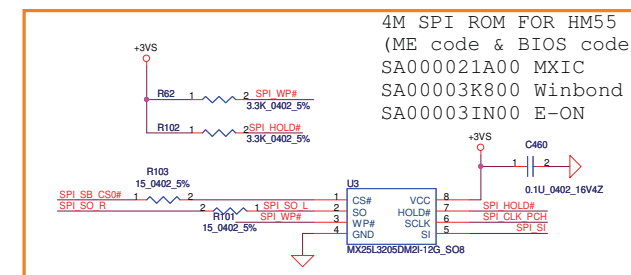
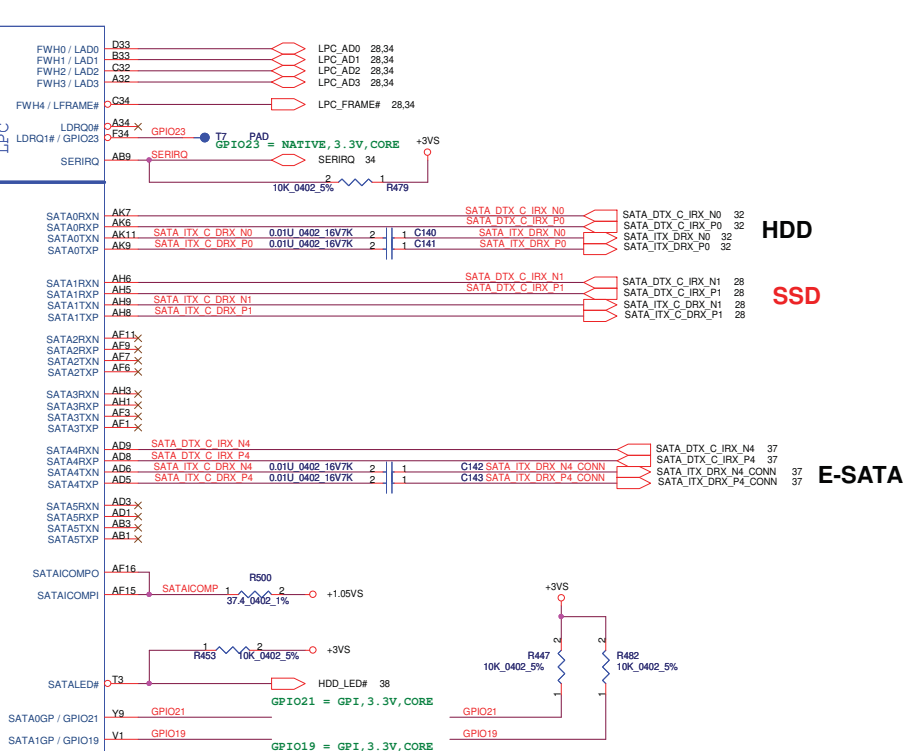
```
GPIO33 = GPO , internal pull-up, should not be pulled low
flash ME core of strap pin pull down
```



PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	★ MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R595	20Kohm	20Kohm	No Install
	R594	10Kohm	10Kohm	No Install

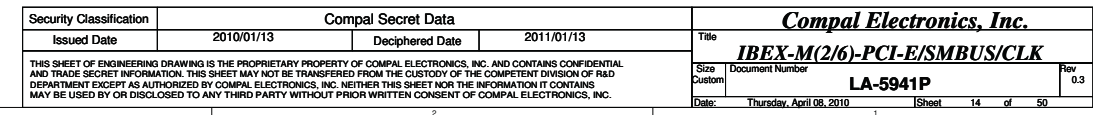


SA00003N7A0 (MP)



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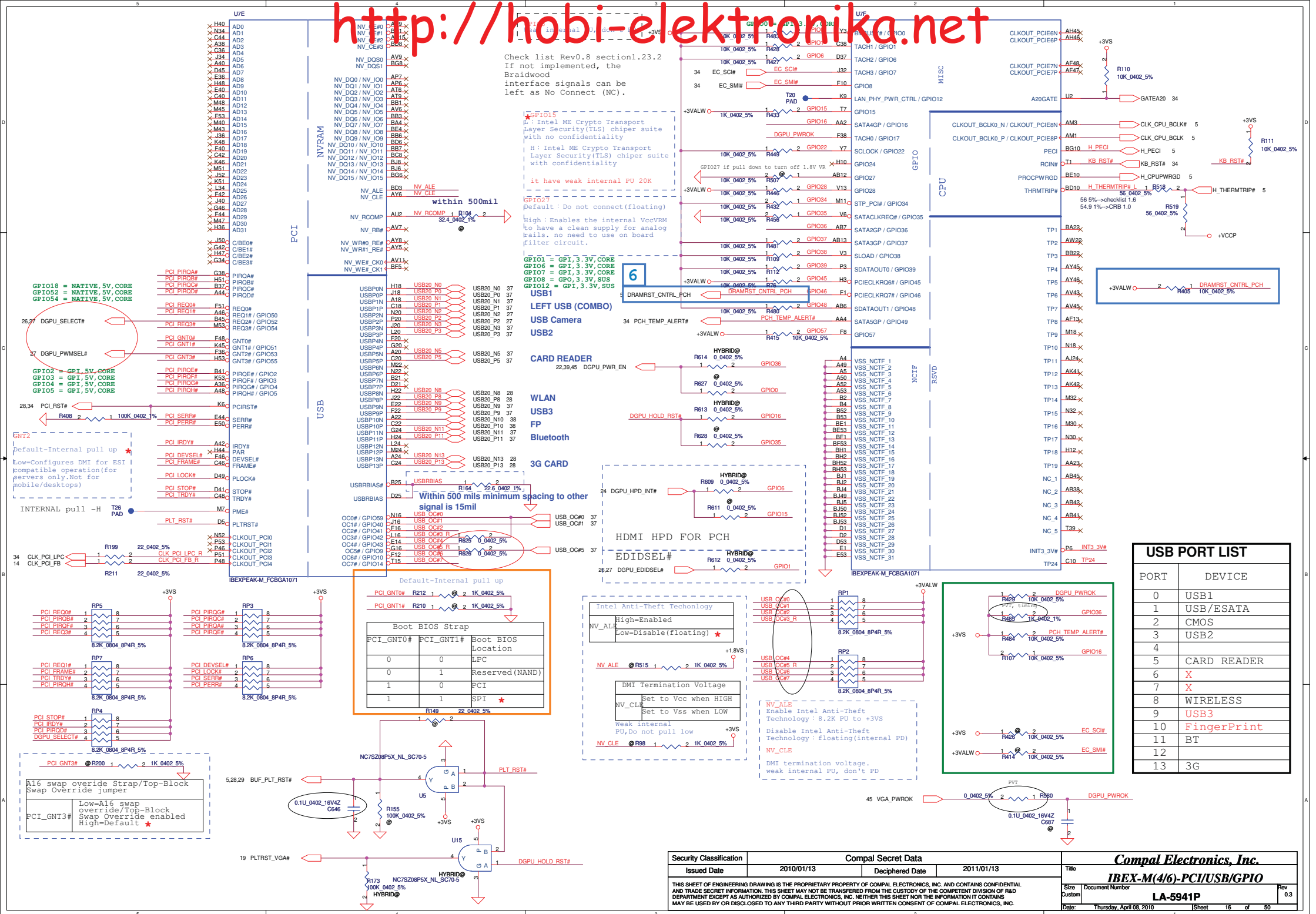
PCIE PORT LIST	
PORT	DEVICE
1	<del>NEW CARD</del>
2	WLAN
3	LAN
4	3G
5	X
6	X
7	X
8	X



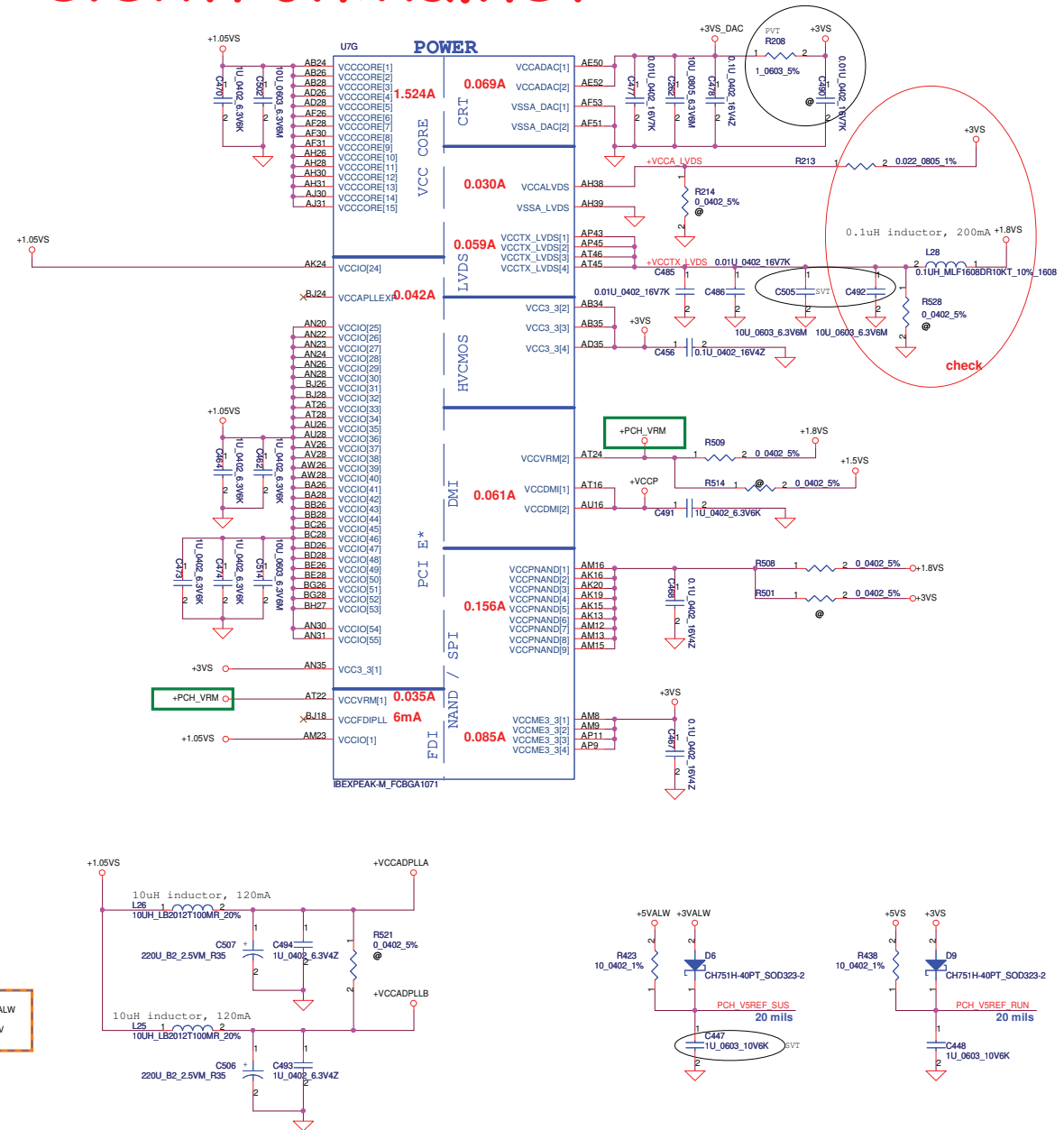
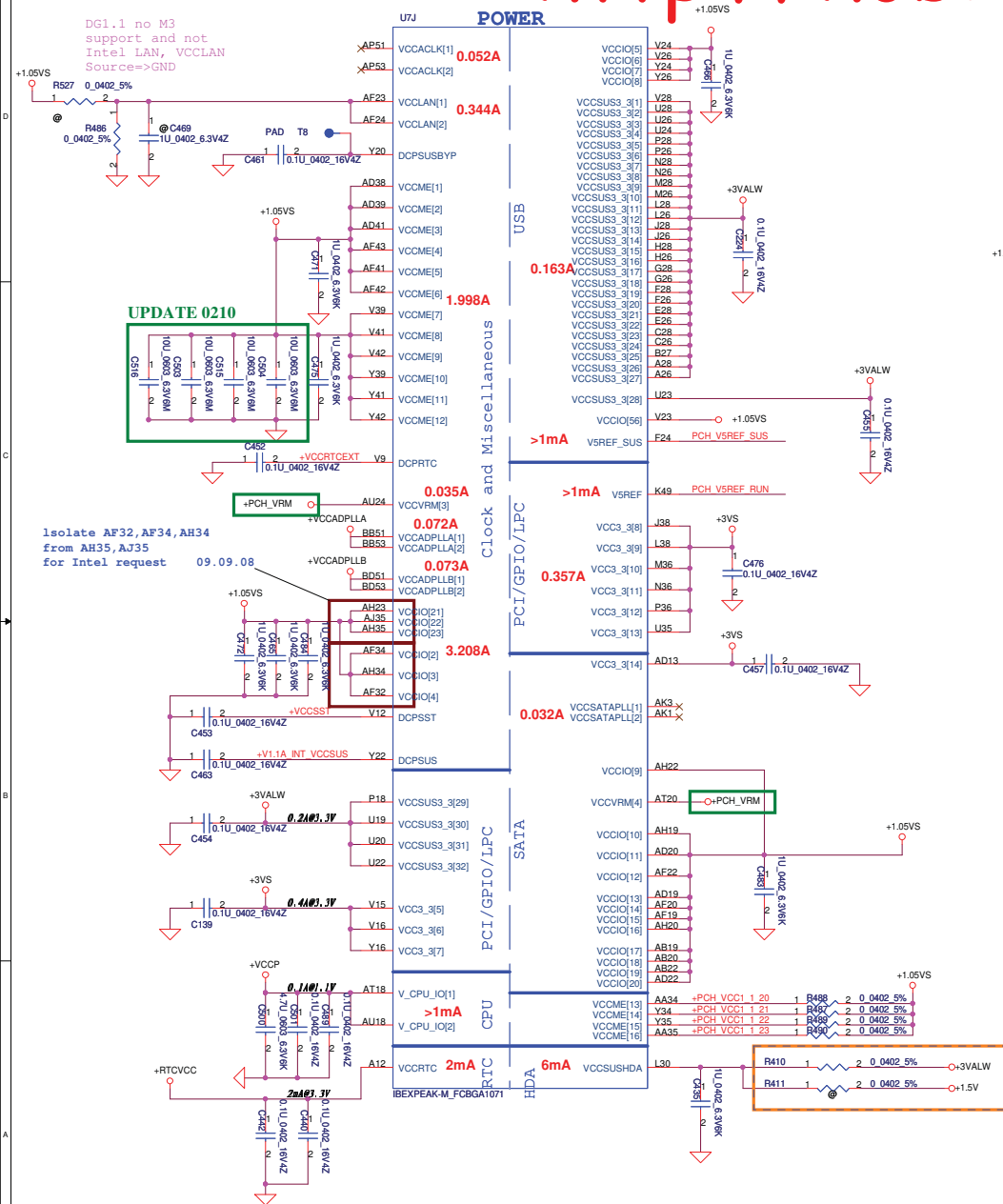




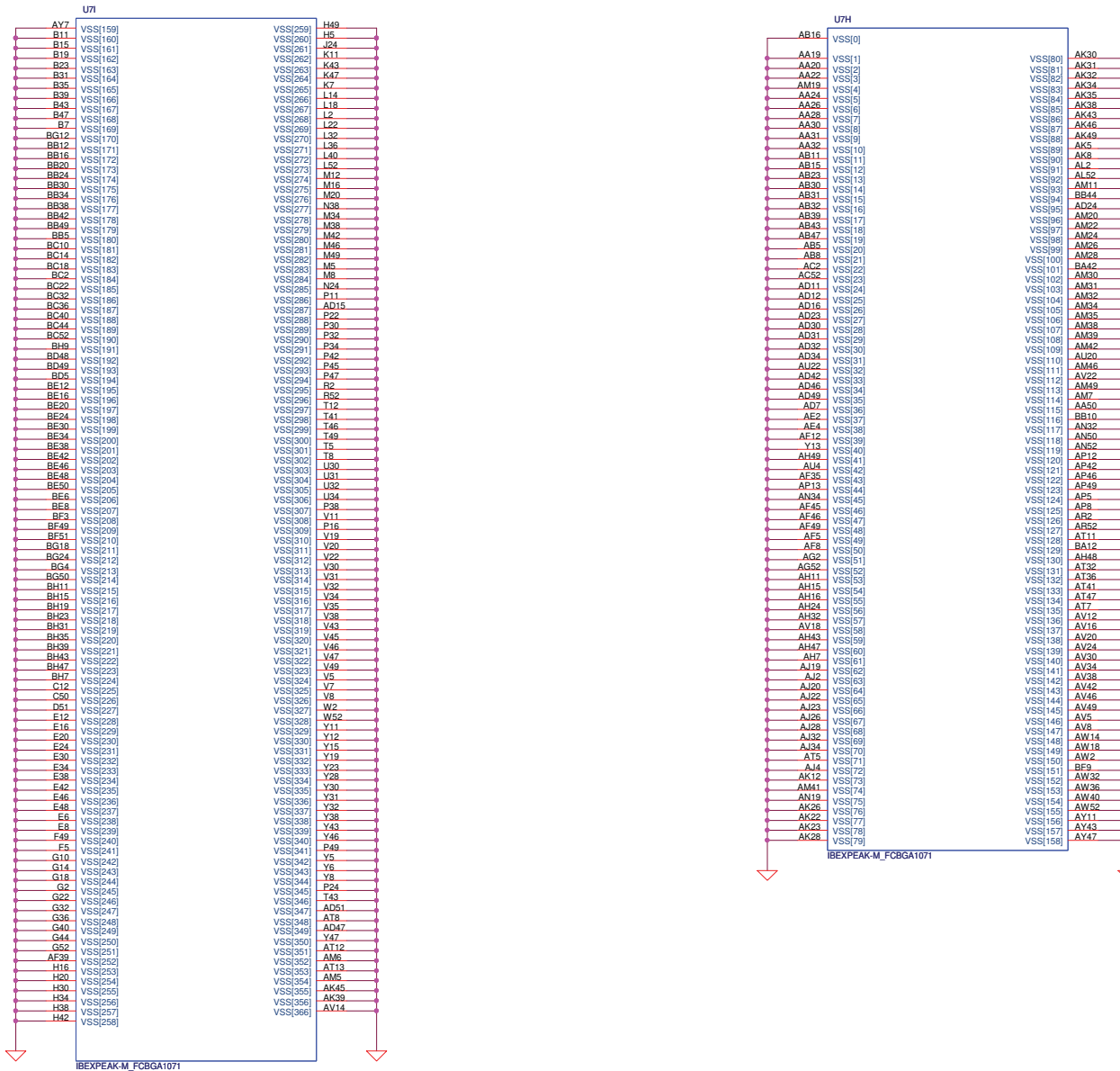




DG1.1 no M3  
support and not  
Intel LAN, VCCLA



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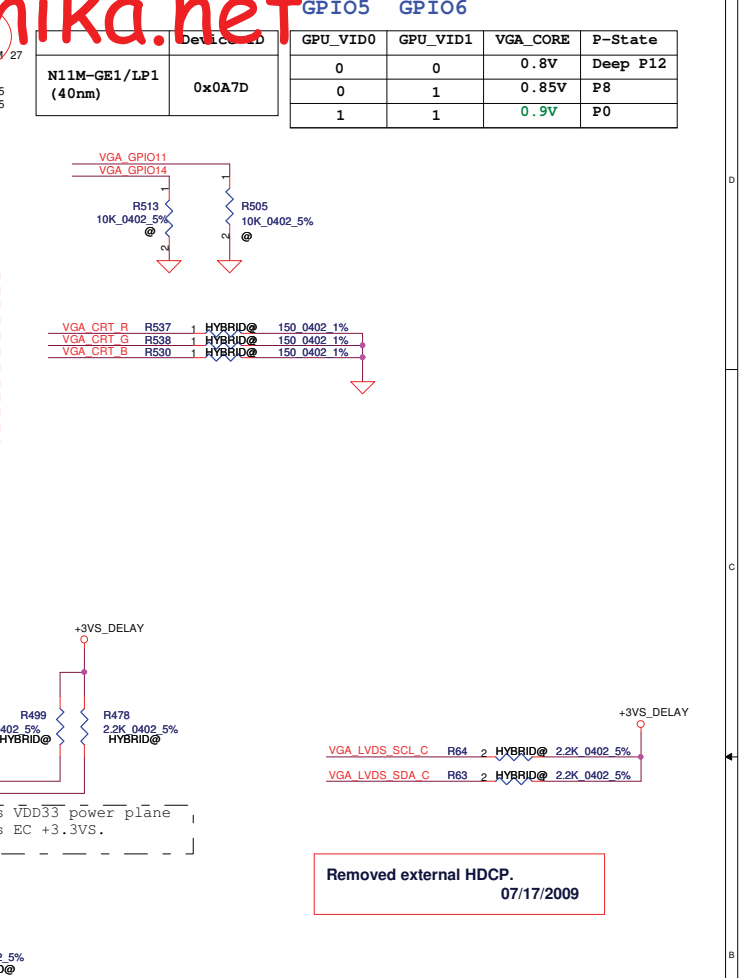
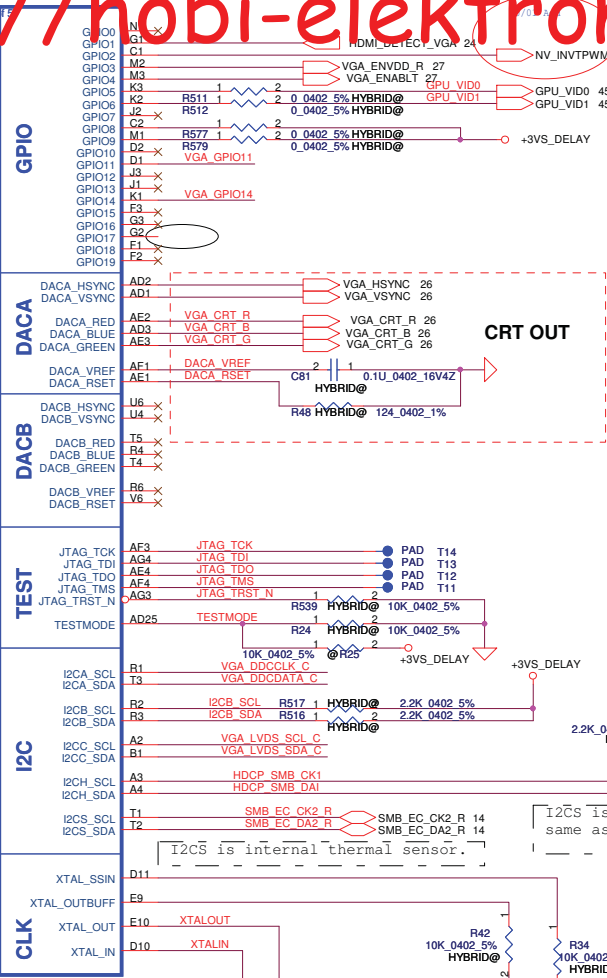
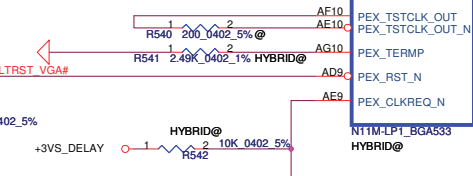
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6	PCIE_CRX_GTX_N0..15]	PCIE_CRX_GTX_N0..15]
6	PCIE_CRX_GTX_P0..15]	PCIE_CRX_GTX_P0..15]

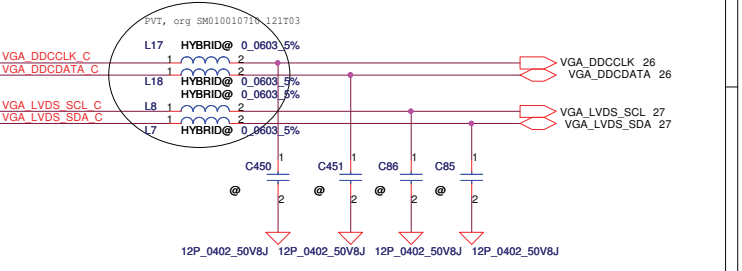
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PCIE_CTX_GRX_N1	AG12	PEX_RX3_N	AG12
PCIE_CTX_GRX_P2	AF13	PEX_RX4_N	AF13
PCIE_CTX_GRX_N2	AE13	PEX_RX5_N	AE13
PCIE_CTX_GRX_P3	AE13	PEX_RX6_N	AE13
PCIE_CTX_GRX_N3	AE13	PEX_RX7_N	AE13
PCIE_CTX_GRX_P4	AG15	PEX_RX8_N	AG15
PCIE_CTX_GRX_N4	AG16	PEX_RX9_N	AG16
PCIE_CTX_GRX_P5	AF18	PEX_RX10_N	AF18
PCIE_CTX_GRX_N5	AF18	PEX_RX11_N	AF18
PCIE_CTX_GRX_P6	AE18	PEX_RX12_N	AE18
PCIE_CTX_GRX_N6	AF18	PEX_RX13_N	AF18
PCIE_CTX_GRX_P7	AG18	PEX_RX14_N	AG18
PCIE_CTX_GRX_N7	AG18	PEX_RX15_N	AG18
PCIE_CTX_GRX_P8	AE19	PEX_RX16_N	AE19
PCIE_CTX_GRX_N8	AE19	PEX_RX17_N	AE19
PCIE_CTX_GRX_P9	AE21	PEX_RX18_N	AE21
PCIE_CTX_GRX_N9	AE21	PEX_RX19_N	AE21
PCIE_CTX_GRX_P10	AG21	PEX_RX20_N	AG21
PCIE_CTX_GRX_N10	AG22	PEX_RX21_N	AG22
PCIE_CTX_GRX_P11	AF22	PEX_RX22_N	AF22
PCIE_CTX_GRX_N11	AE22	PEX_RX23_N	AE22
PCIE_CTX_GRX_P12	AG24	PEX_RX24_N	AG24
PCIE_CTX_GRX_N12	AG24	PEX_RX25_N	AG24
PCIE_CTX_GRX_P13	AE25	PEX_RX26_N	AE25
PCIE_CTX_GRX_N13	AG25	PEX_RX27_N	AG25
PCIE_CTX_GRX_P14	AG26	PEX_RX28_N	AG26
PCIE_CTX_GRX_N14	AG26	PEX_RX29_N	AG26
PCIE_CTX_GRX_P15	AE27	PEX_RX30_N	AE27
PCIE_CTX_GRX_N15	AE27	PEX_RX31_N	AE27

PCIE_CRX_GTX_P0	C120	HYBRID@	2	0.1U	0.402	16V7K
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PCIE_CRX_GTX_N4	C115	HYBRID@	2	0.1U	0.402	16V7K
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PCIE_CRX_GTX_N7	C108	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P8	C107	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N8	C105	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P9	C104	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N9	C103	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P10	C102	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N10	C101	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P11	C100	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N11	C99	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P12	C98	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N12	C97	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P13	C96	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N13	C95	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P14	C94	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N14	C93	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_P15	C92	HYBRID@	2	0.1U	0.402	16V7K
PCIE_CRX_GTX_N15	C91	HYBRID@	2	0.1U	0.402	16V7K

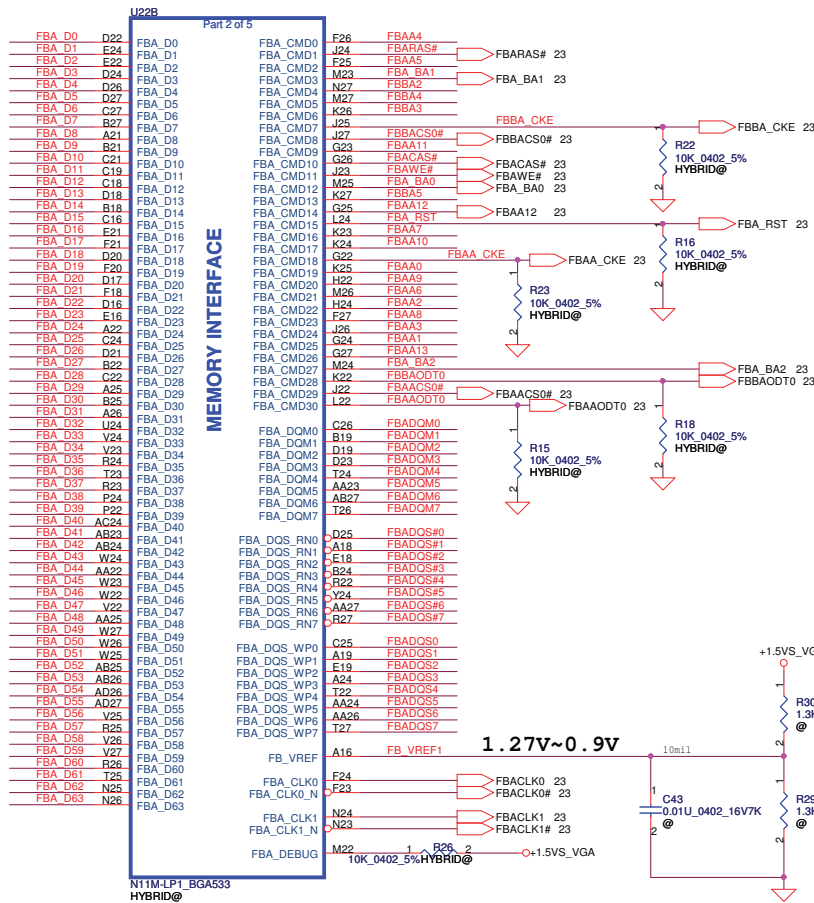
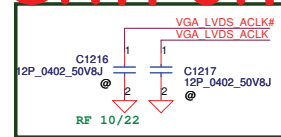
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14	CLK_PCIE_VGA#	CLK_PCIE_VGA#	AC10

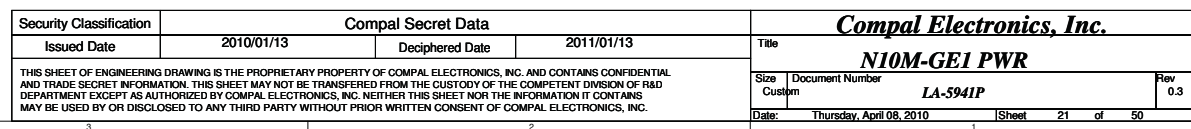


Removed external HDCP.  
07/17/2009









A total of 8 signals are required for SB1, trapping this includes



DG-04642-001-V01(May 22, 2009)

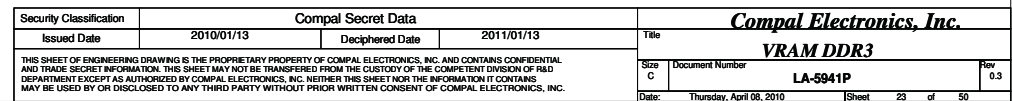
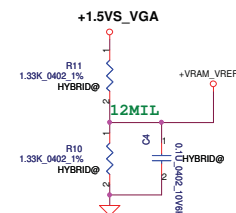
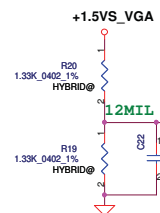
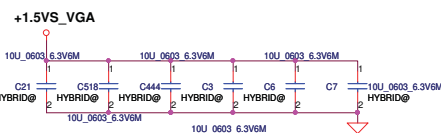
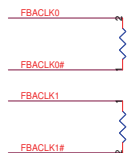


STRAP1 use for 3GIO\_PADCFG to set 35K pull up.  
(PUN-04335-001\_V10 HW9 update)

x79

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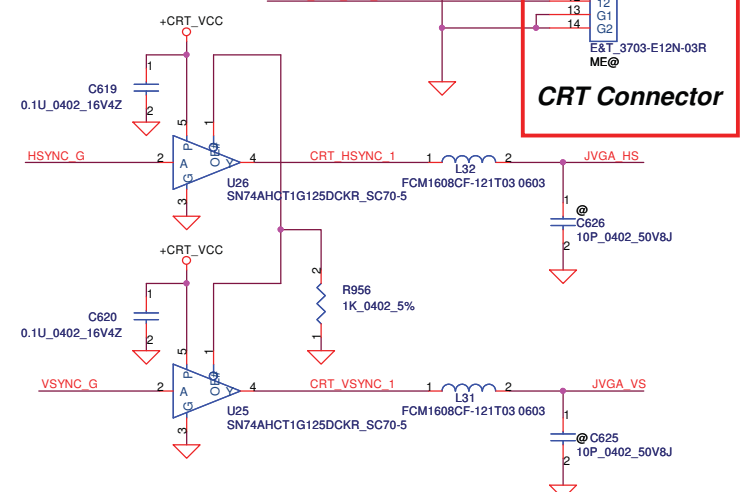
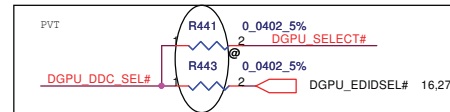
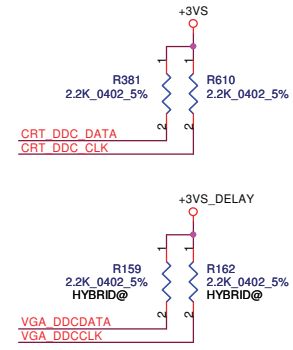
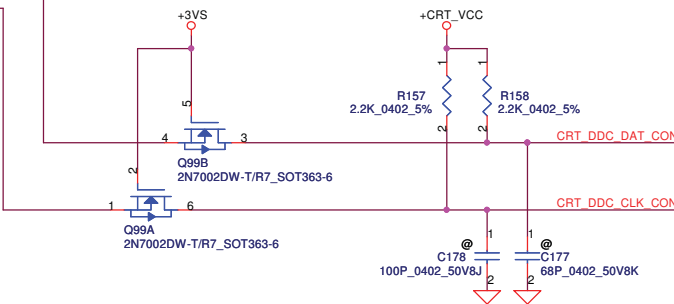
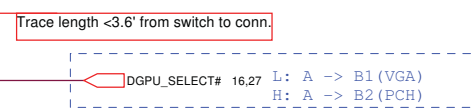
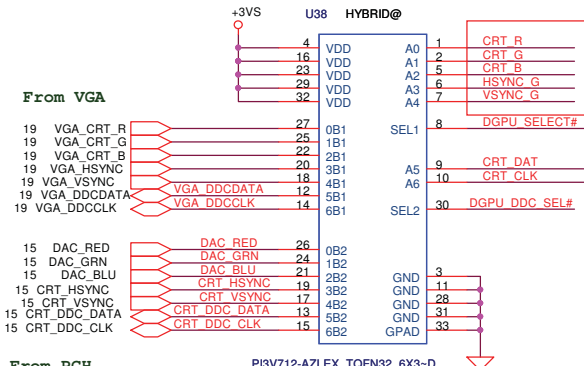
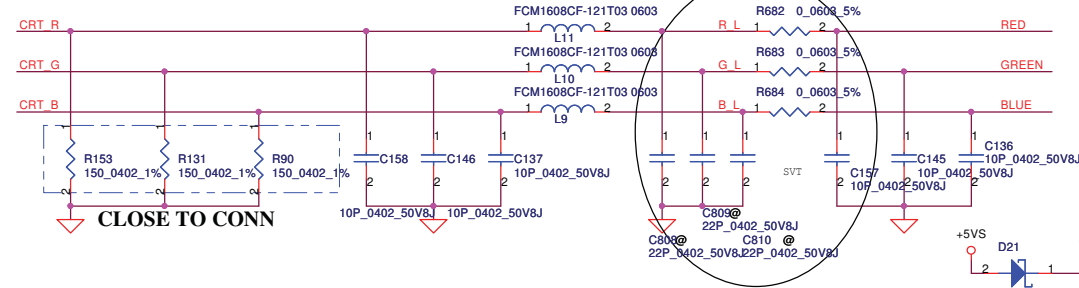
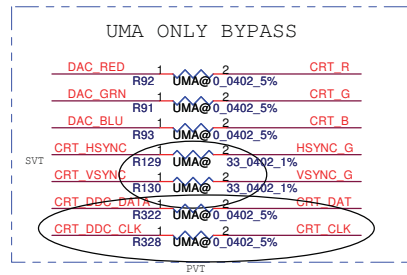


RESERVE THE R668 PULL UP TO 3VS  
RESERVE THE R670 PULL DOWN TO GND  
CHANGE R245 FROM 499 TO 3.4K OHM

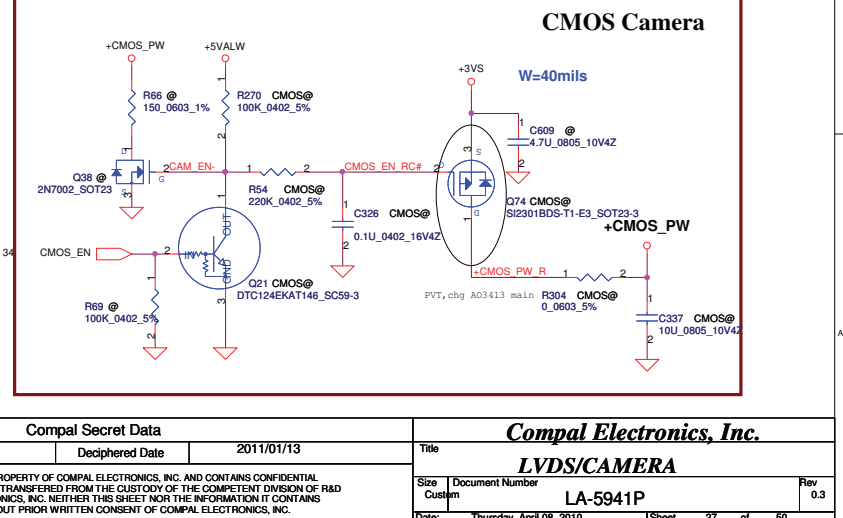
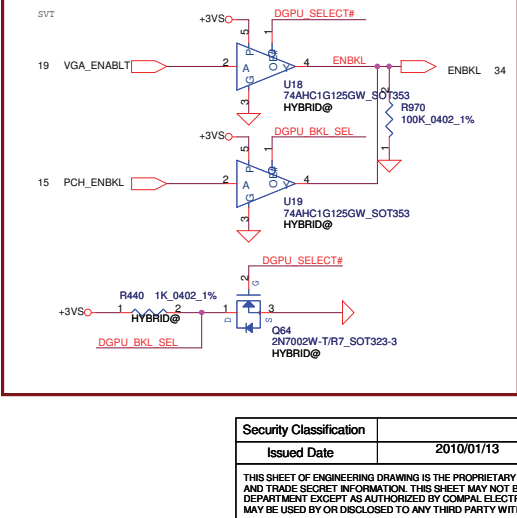
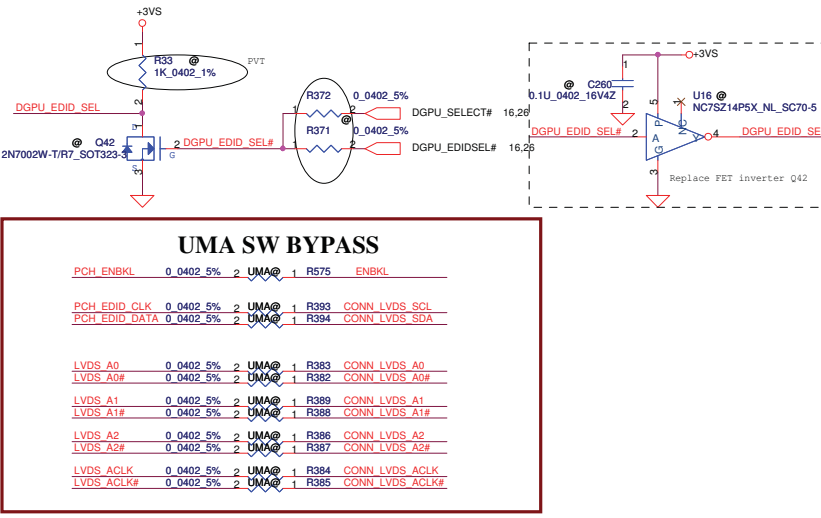
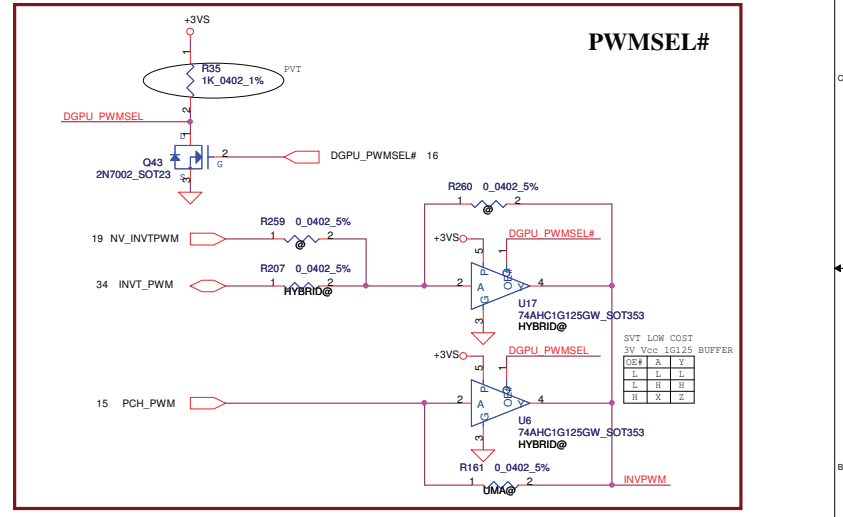
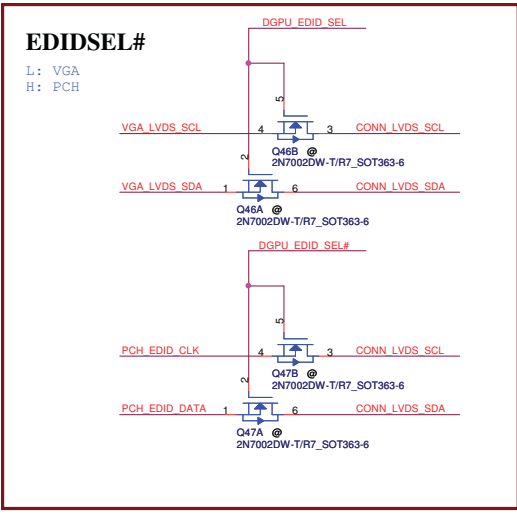
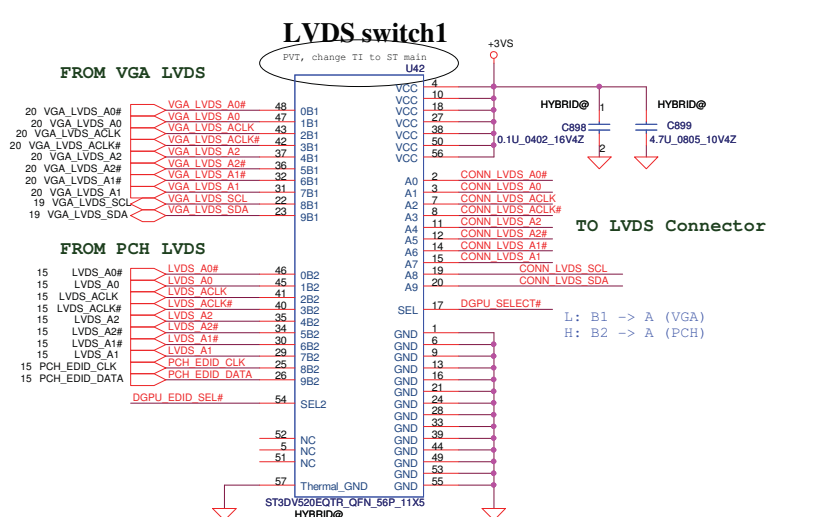
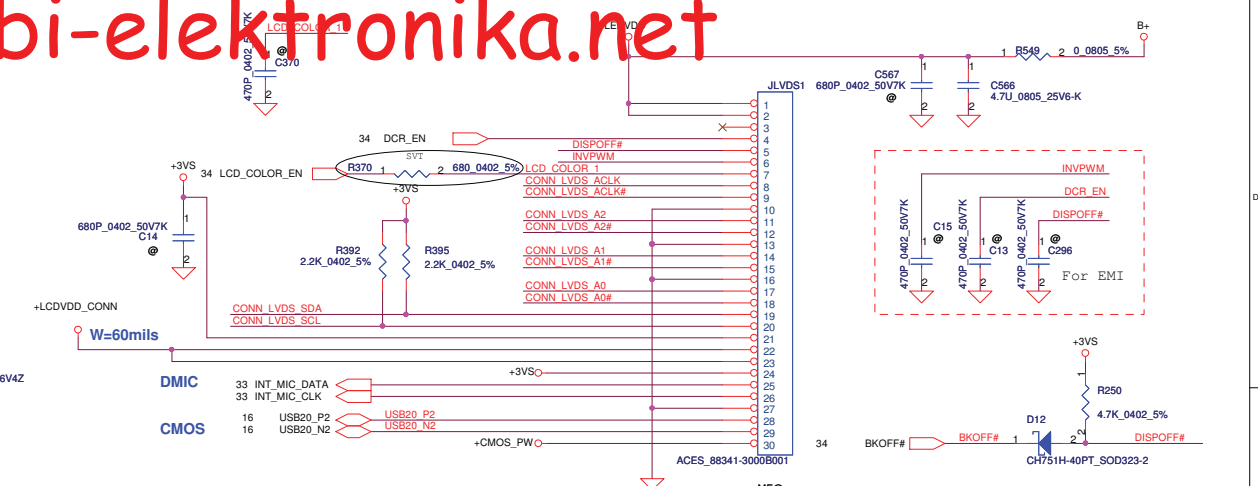
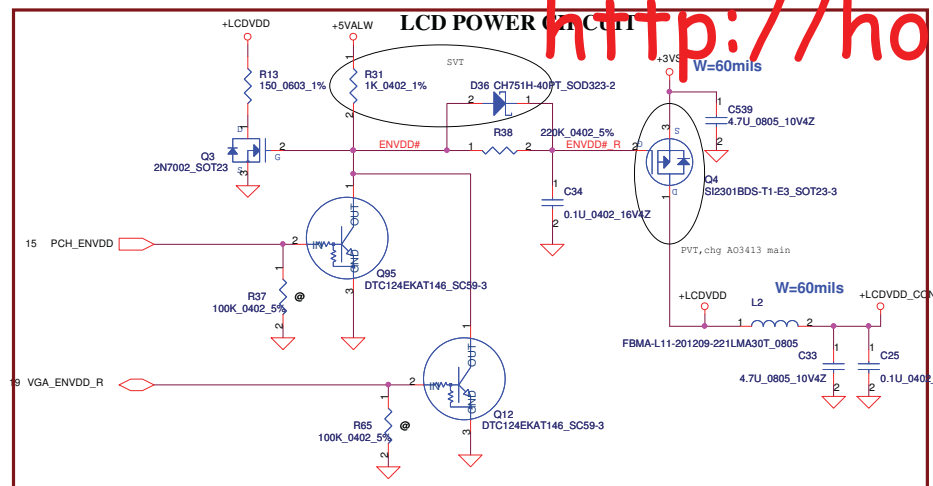


Pin1	R331	NC
Pin3	R248,R334	NC
Pin4	R246,R247	NC
Pin6	R245	499ohm
Pin11	R332	NC
Pin12	R280	NC
Pin27	R261	NC
Pin33	R333	NC
Pin34	R254	4.7K ohm

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				Level Shifter _ASM1442				
				Size	Document Number		Rev 0.3	
				Custom	LA-5941P			
Date: Thursday, April 08, 2010				Sheet	25	of 50		

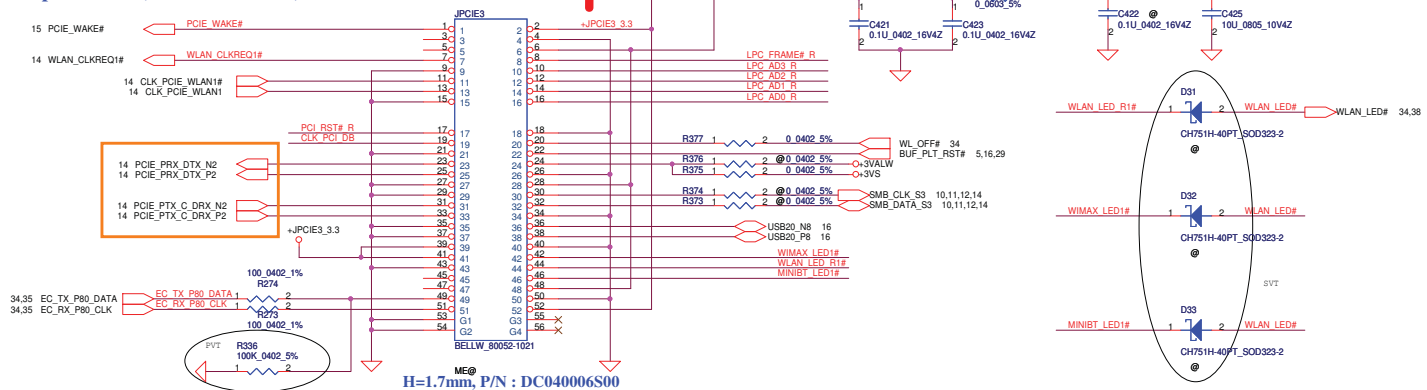


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Size	Custom	Document Number	LA-5941P		Rev 0.3
Date:	Thursday, April 08, 2010	Sheet	26	of	50



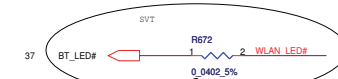
Mini-Express Card for WLAN/WiMAX(Ha) <http://hobi-elektronika.net>

### Mini-Express Card(WLAN/WiMAX)

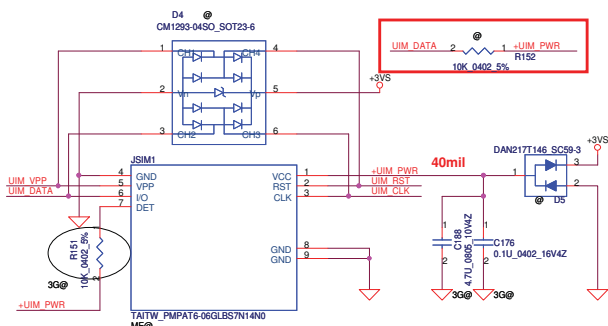
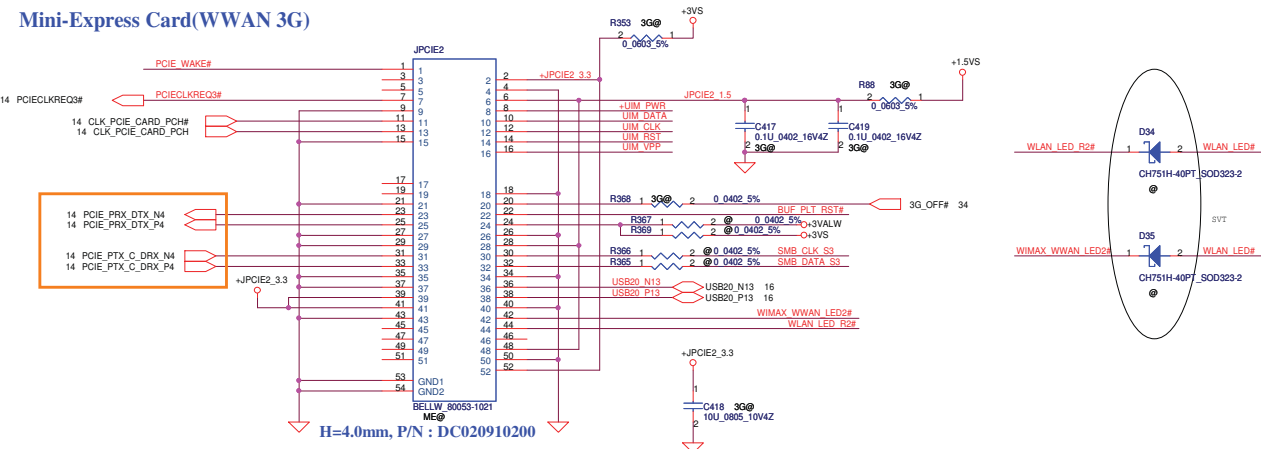


**Reserve for SW mini-pcie debug card.**

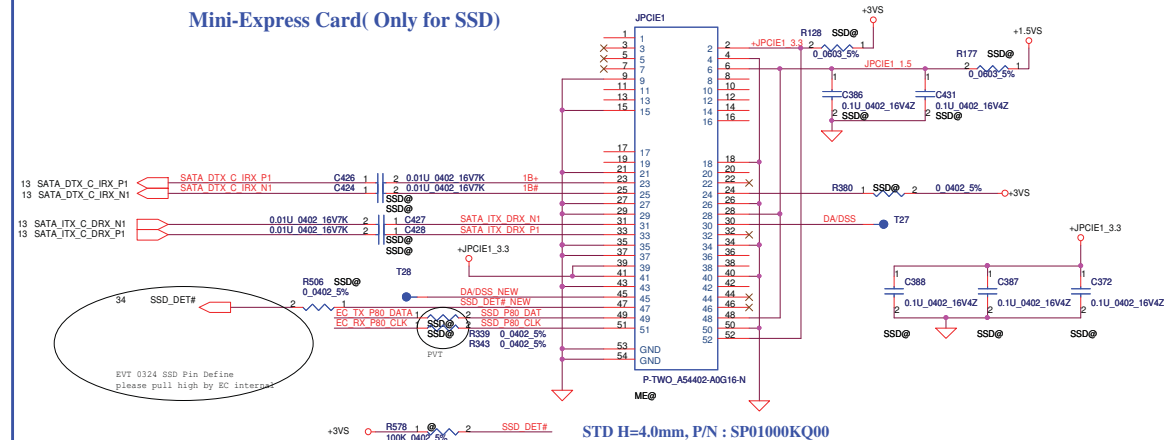
**Series resistors closed to KBC side.**



### Mini-Express Card(WWAN 3G)



### Mini-Express Card( Only for SSD)

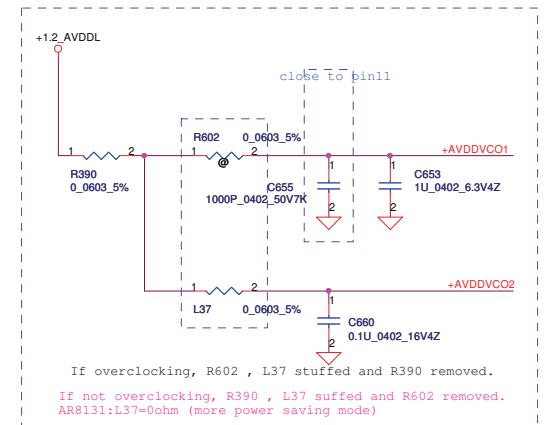
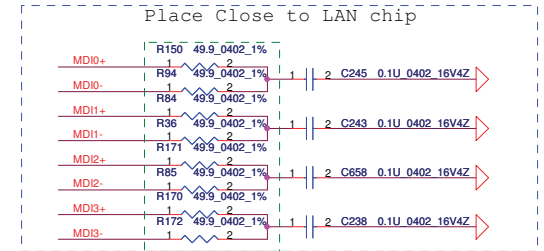
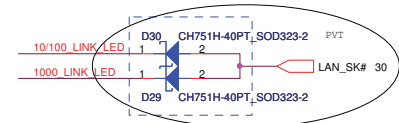
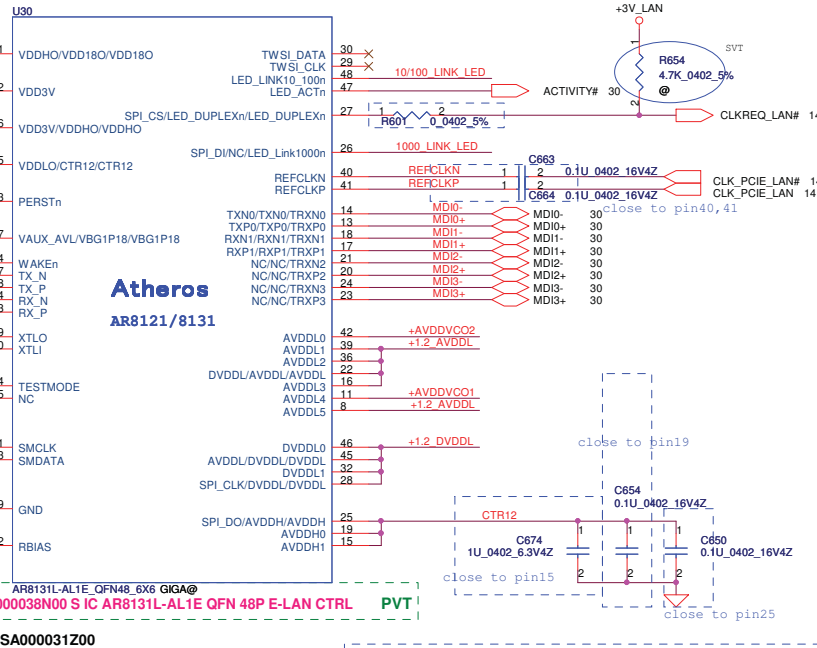
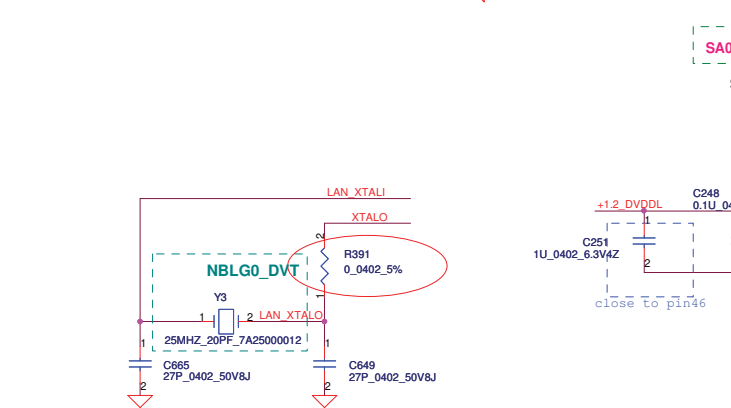
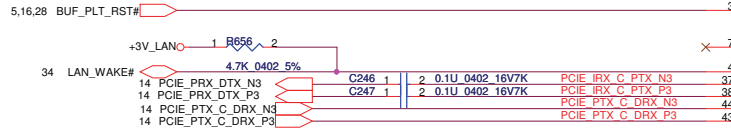
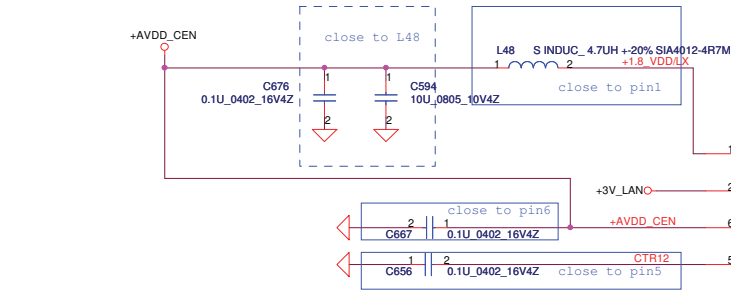
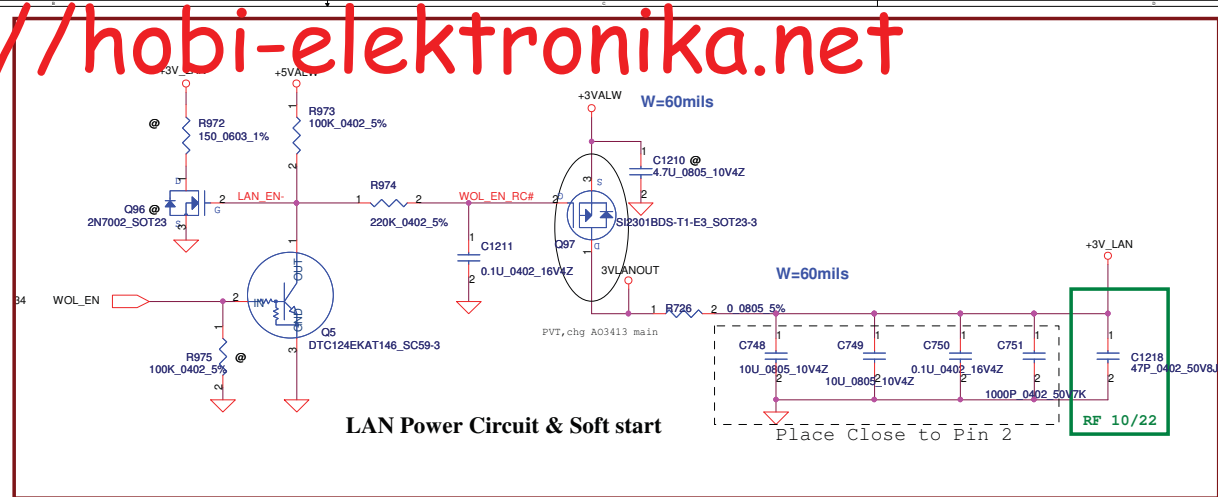


## SSD Pin Table

Pin Number	SATA Assignment
11	
13	
17	
19	
23	+B (port 1)
25	-B (port 1)
30	45 DA/DSS DA/DSS (NEW)
31	-A (port 1)
32	47 SSD_DET# SSD_DET# (NEW)
33	+A (port 1)

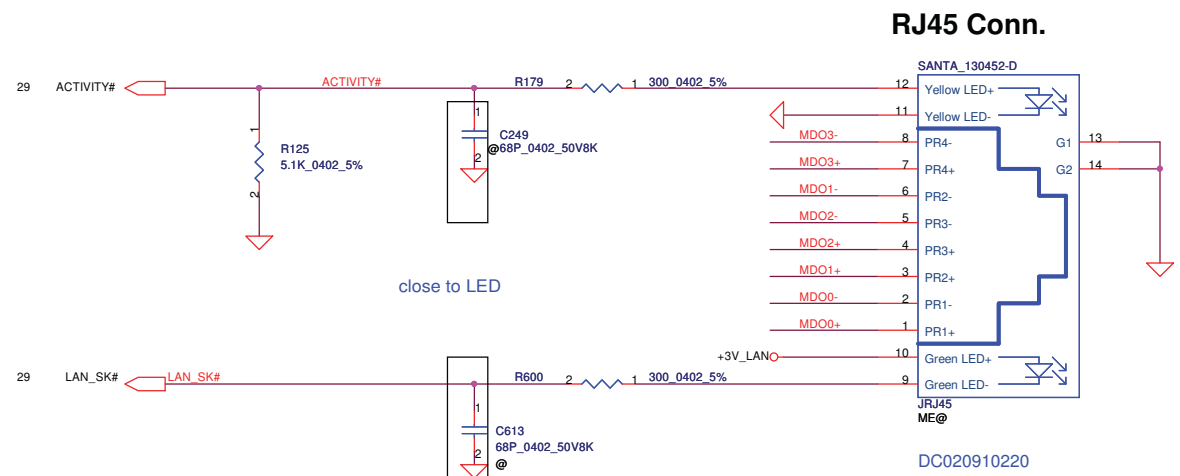
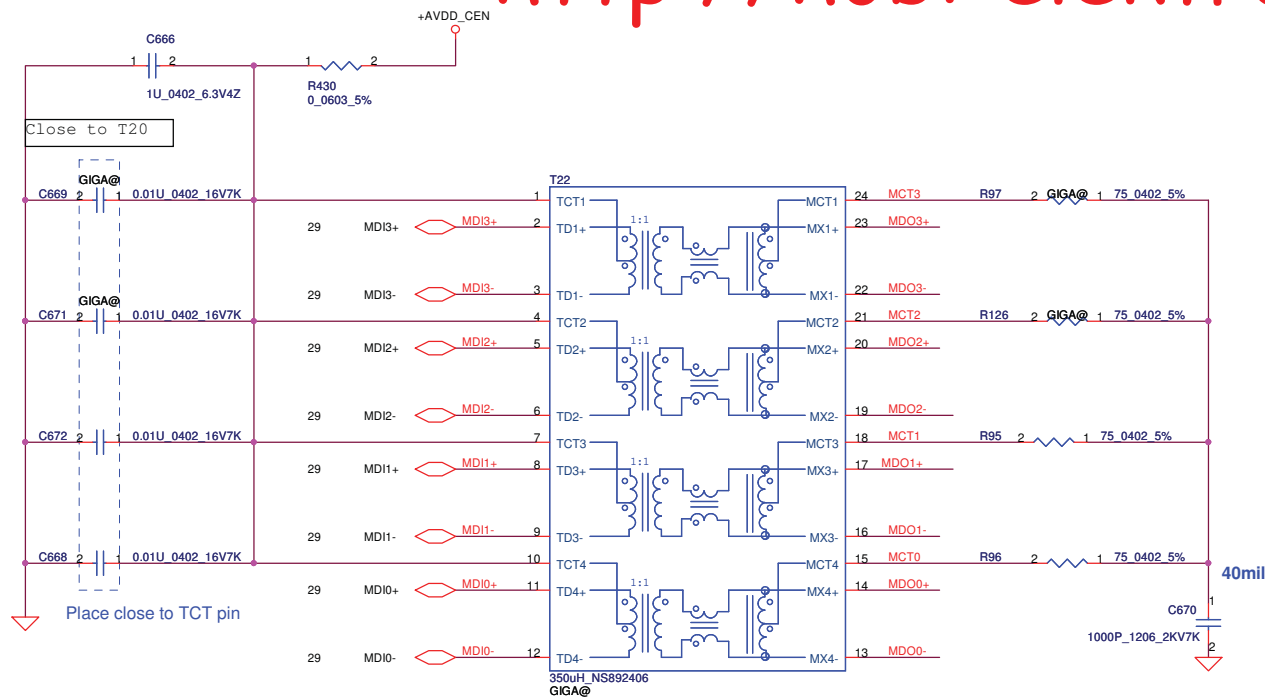
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				Size	Document Number	Rev
				LA-5941P		0.3
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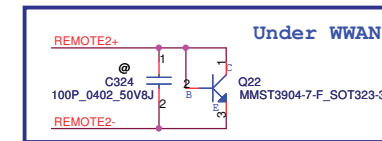
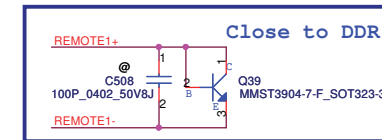
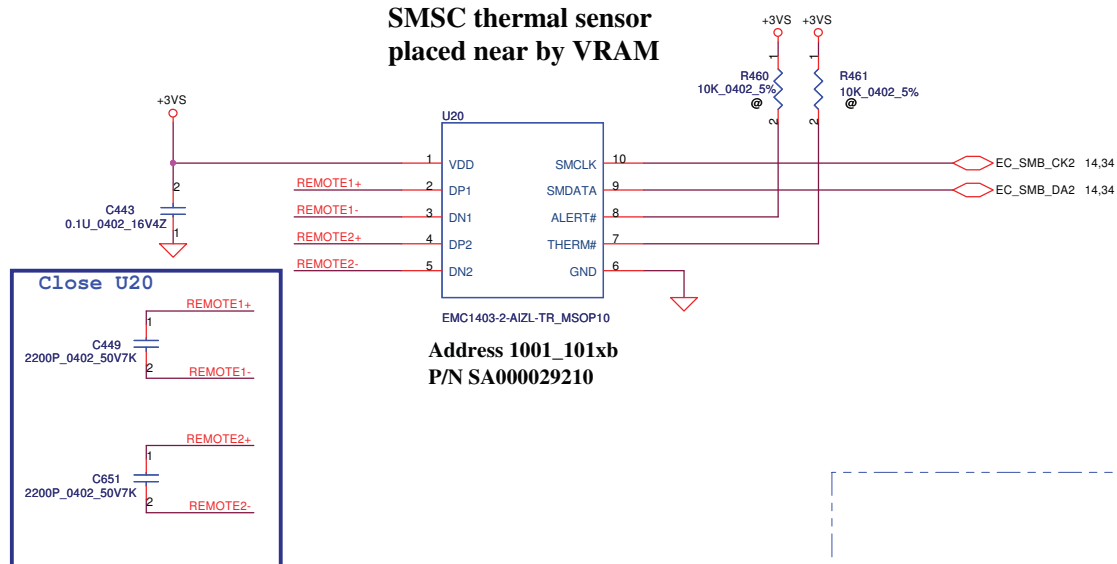
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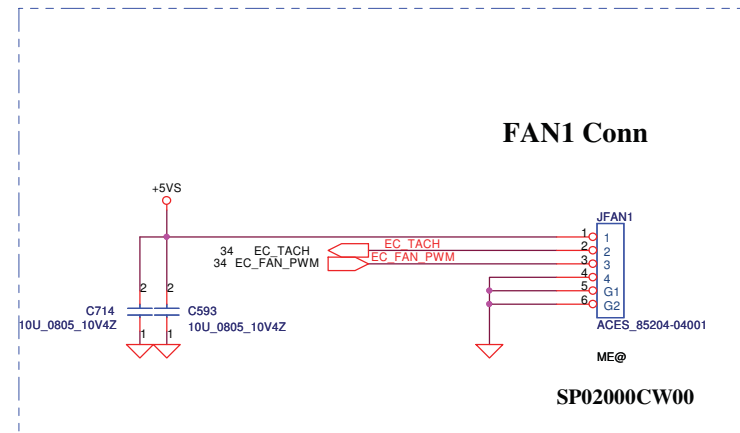


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				Date: Thursday, April 08, 2010	Sheet 30 of 50

## SMSC thermal sensor placed near by VRAM

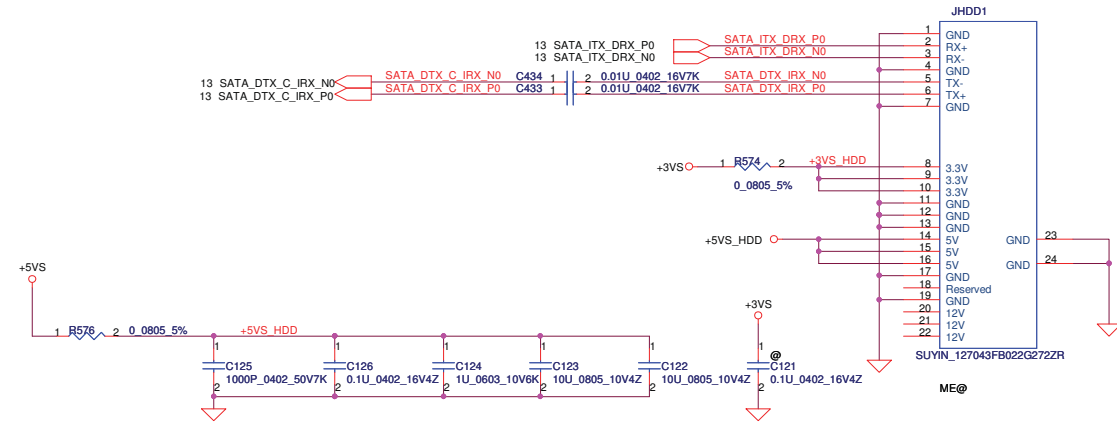


REMOTE1, 2+/-:  
Trace width/space: 10/10 mil  
Trace length: <8"

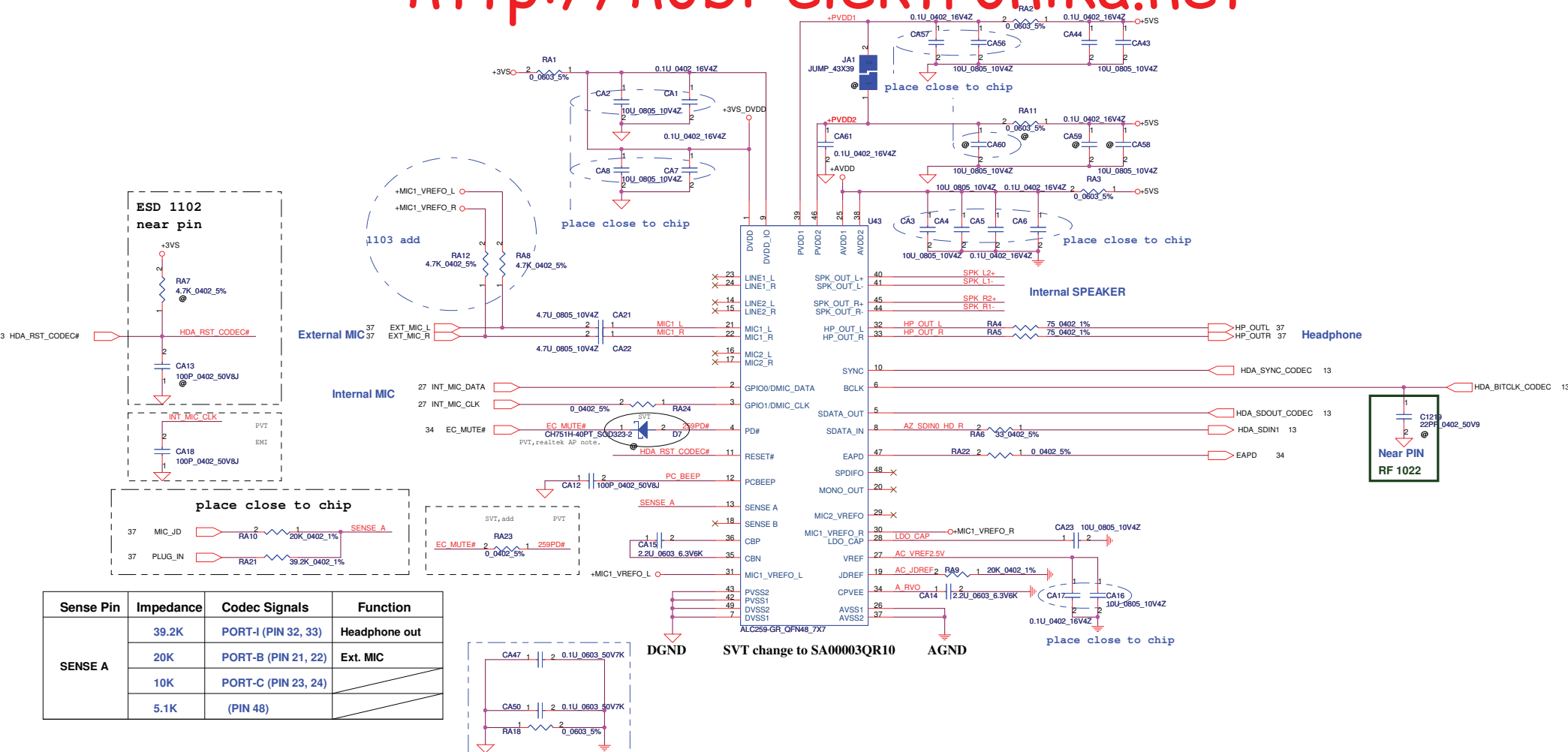


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				Date: Thursday, April 08, 2010	Sheet 31 of 50

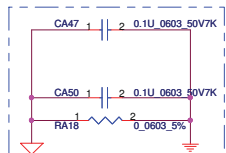
## SATA HDD Conn.



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Issued Date	2010/01/13	Deciphered Date	2011/01/13	HDD/ODD Connector	
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

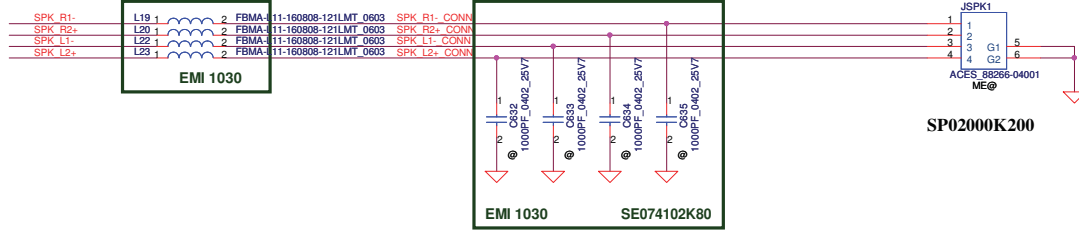


### PC BEEP

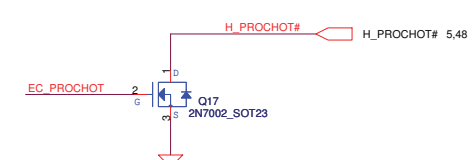
### EC BEEP

### ICH BEEP

wide 20MIL



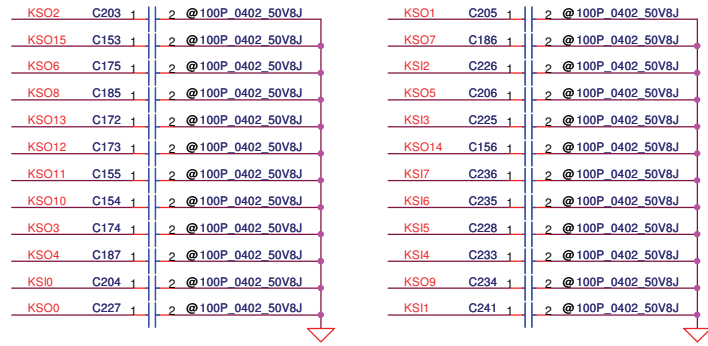
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Date: Thursday, April 08, 2010				Sheet 33 of 50	Rev 0.3



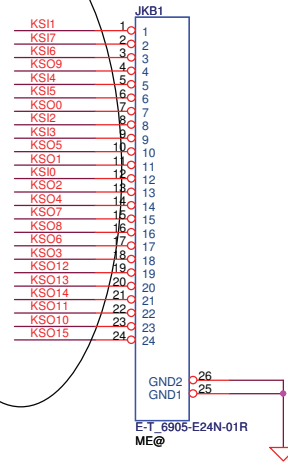
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					Size	Document Number		Rev
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					Date:	Thursday, April 08, 2010		Sheet

## INT\_KBD Conn.

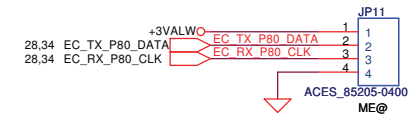
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KSO[0..15] 34



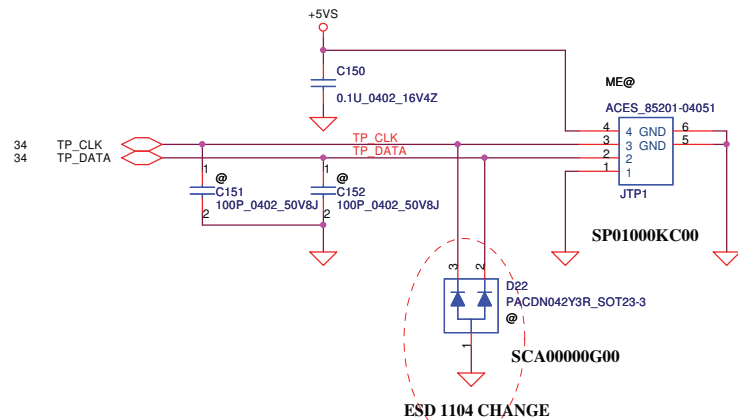
## KB Matrix 10/30



## EC DEBUG PORT

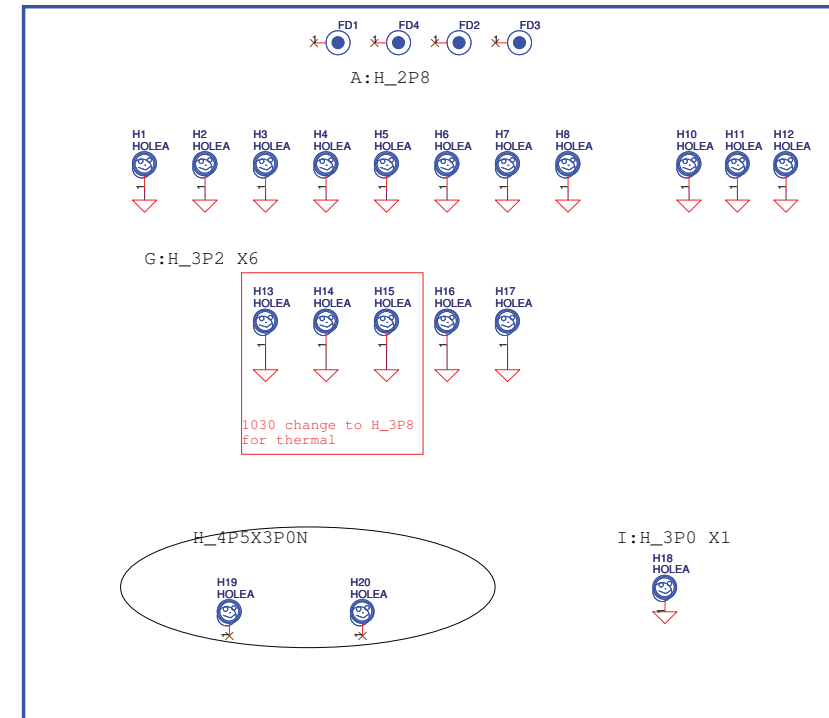
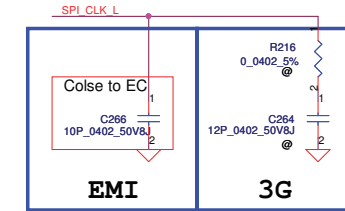
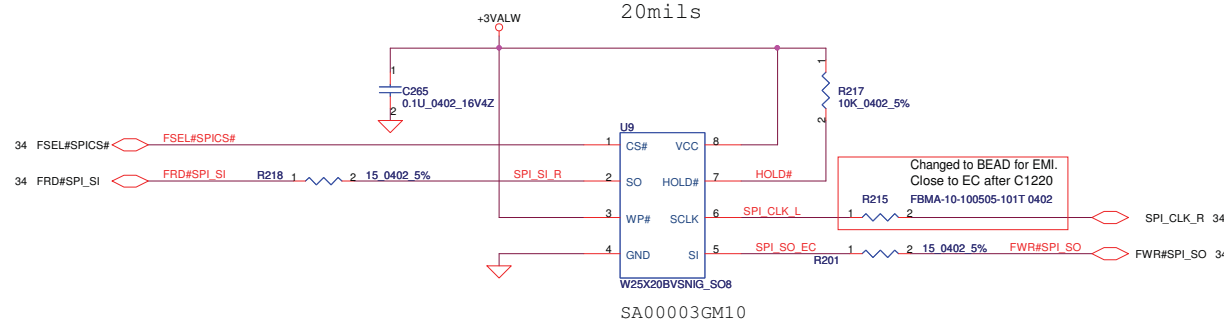


## To TP/B Conn.



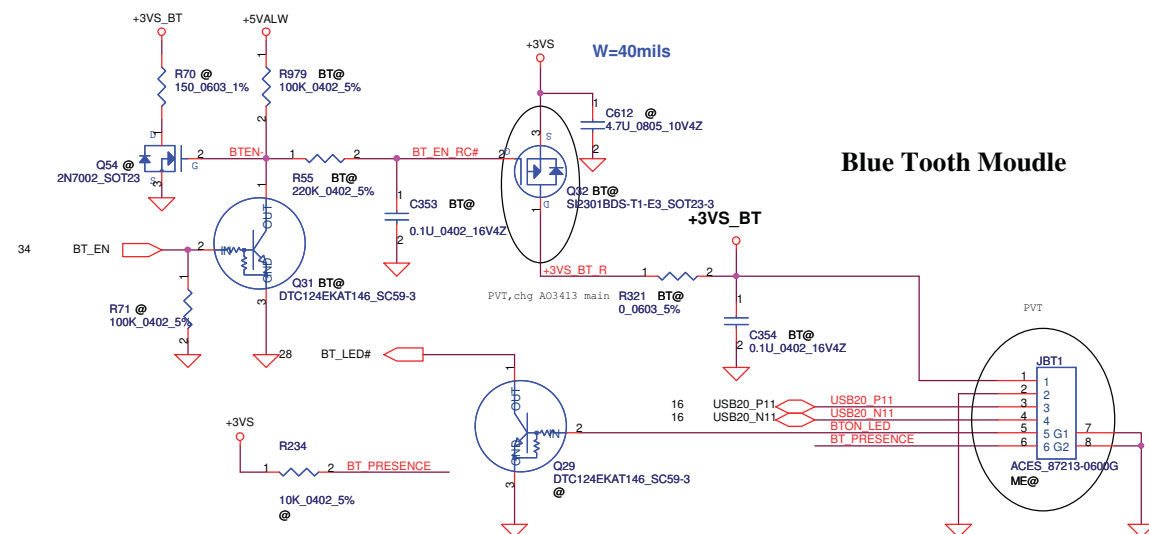
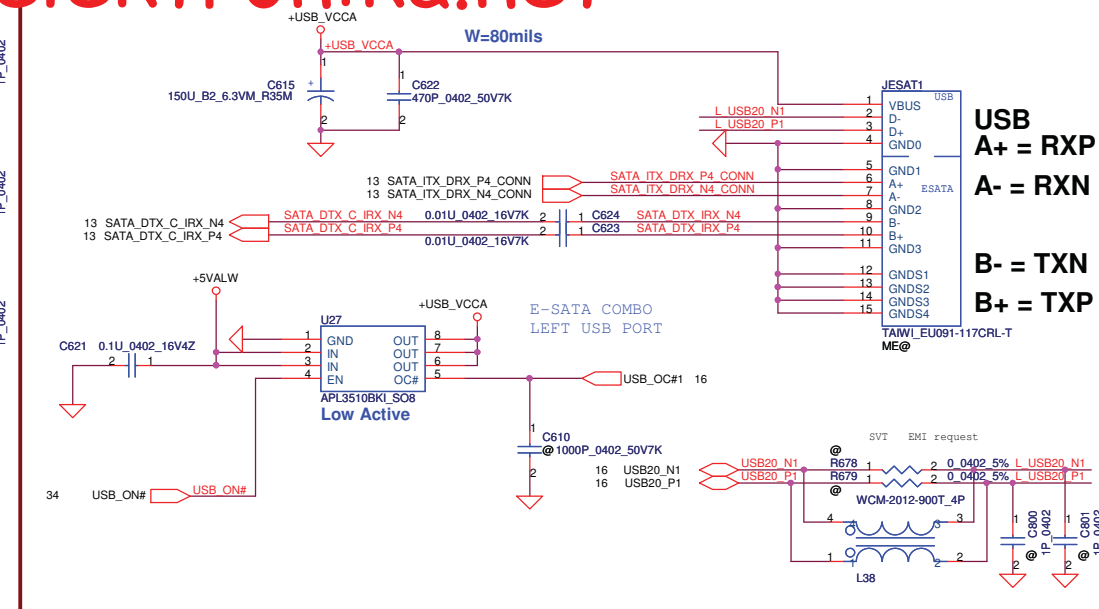
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Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title	
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## FOR EC 256KB SPI ROM (150mil PACKAGE)



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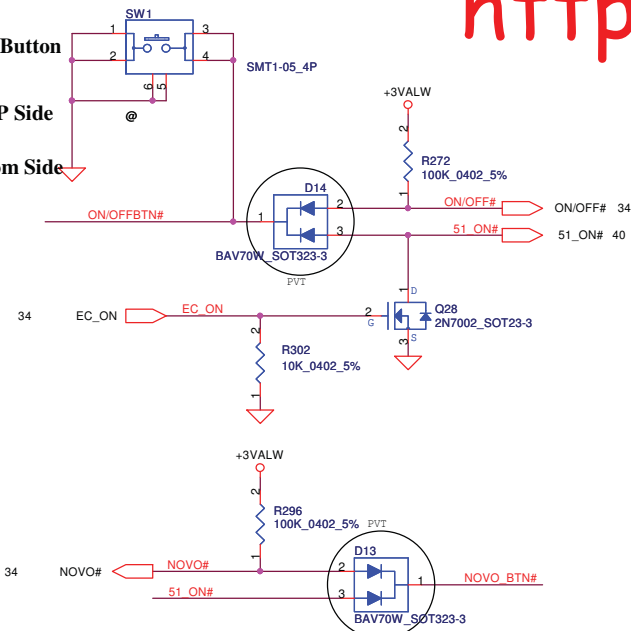
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# ON/OFF switch FOR DEBUG

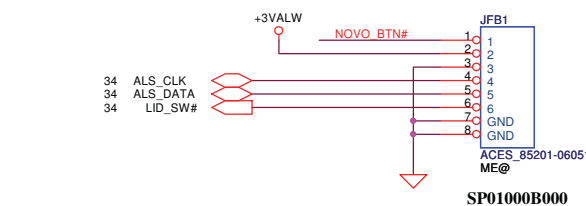
## Power Button

TOP Side

Bottom Side

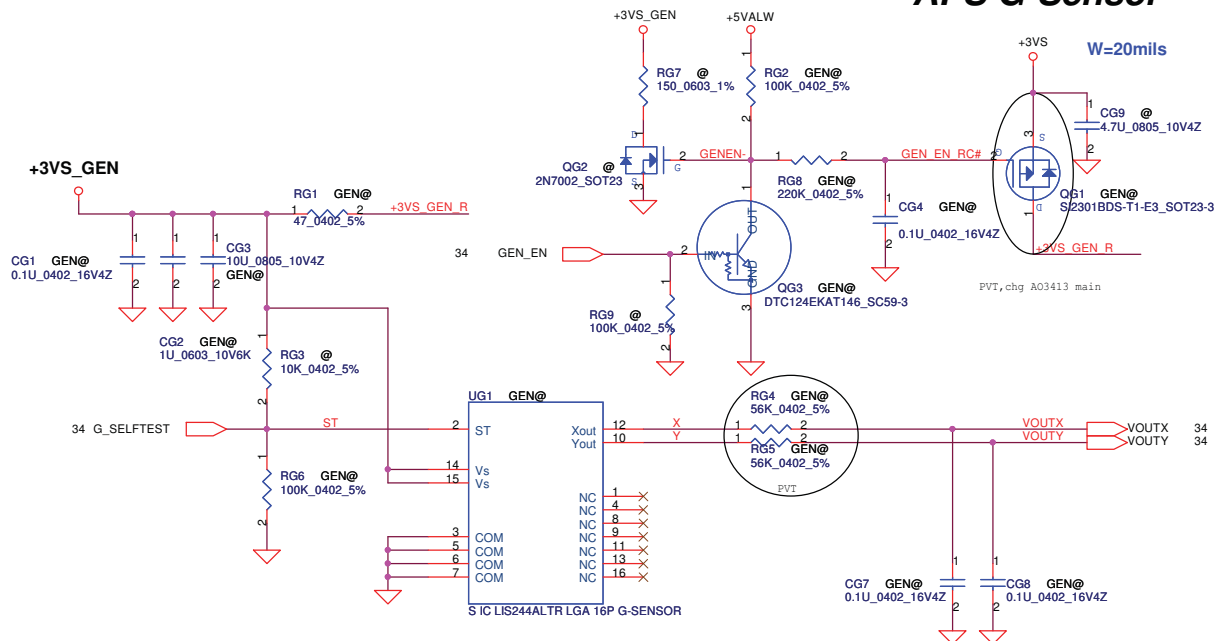


## NOVOBottom/ALS Board Conn.6pin



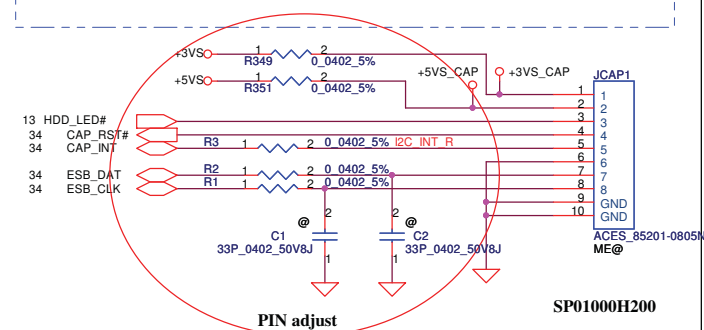
EMI REQUEST 1ST = SCA00000E00  
2ST = SCA00000R00

## APS G-Sensor

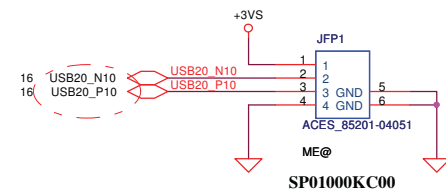


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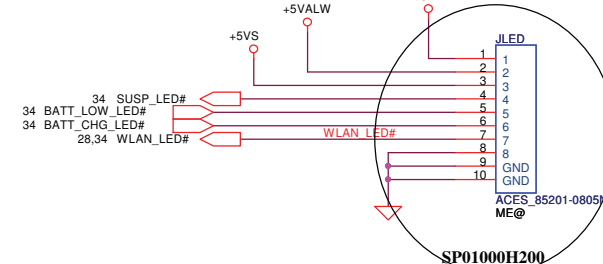
## Cip Sensor Board Conn. 8pin ENE SB3534



## FP Board Conn 4 pin



## LED CONN 8 pin

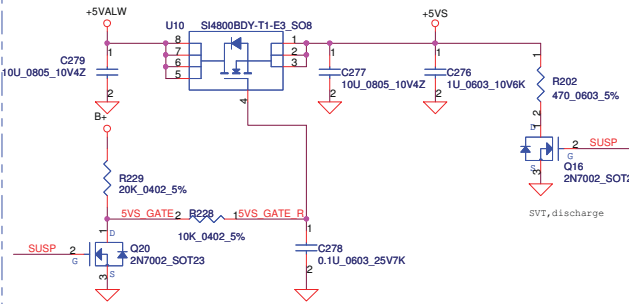


Amber  
Blue

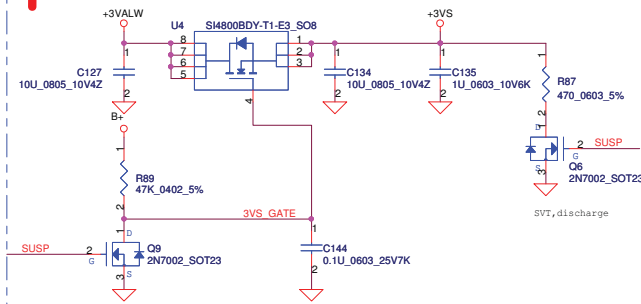


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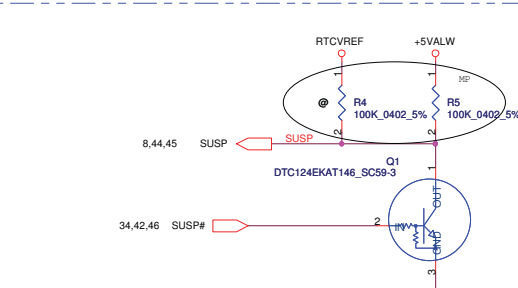
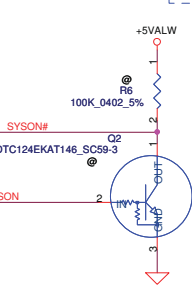
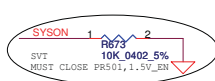
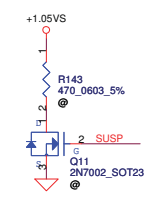
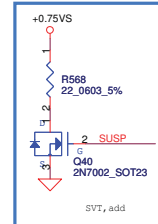
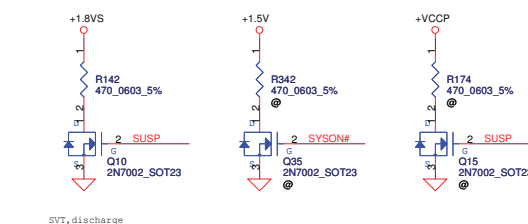
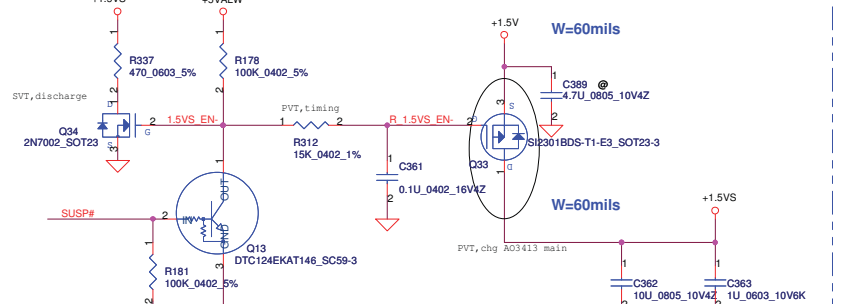
### +5VALW TO +5VS



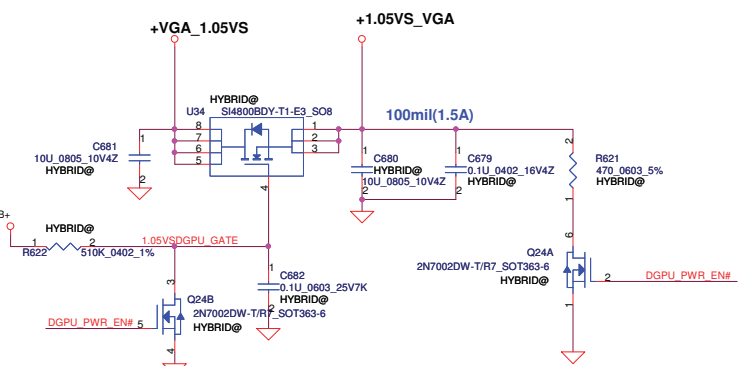
### +3VALW TO +3VS



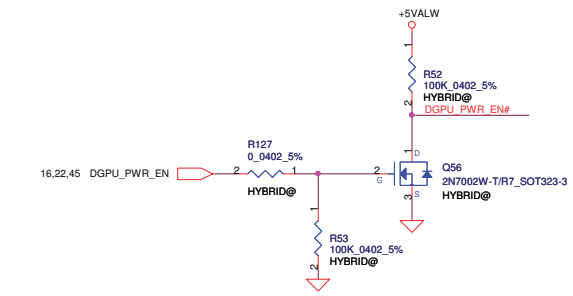
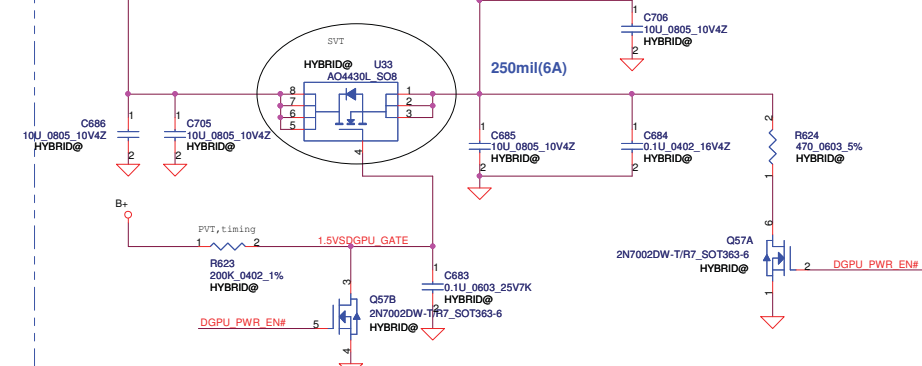
### +1.5V TO +1.5VS



### +1.05VS to +1.05VS\_VGA Transfer



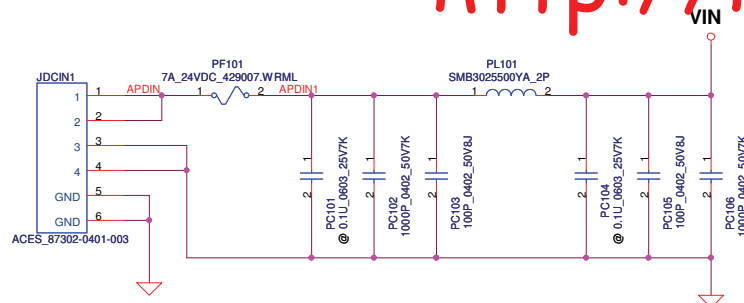
### +1.5V to +1.5VS\_VGA Transfer



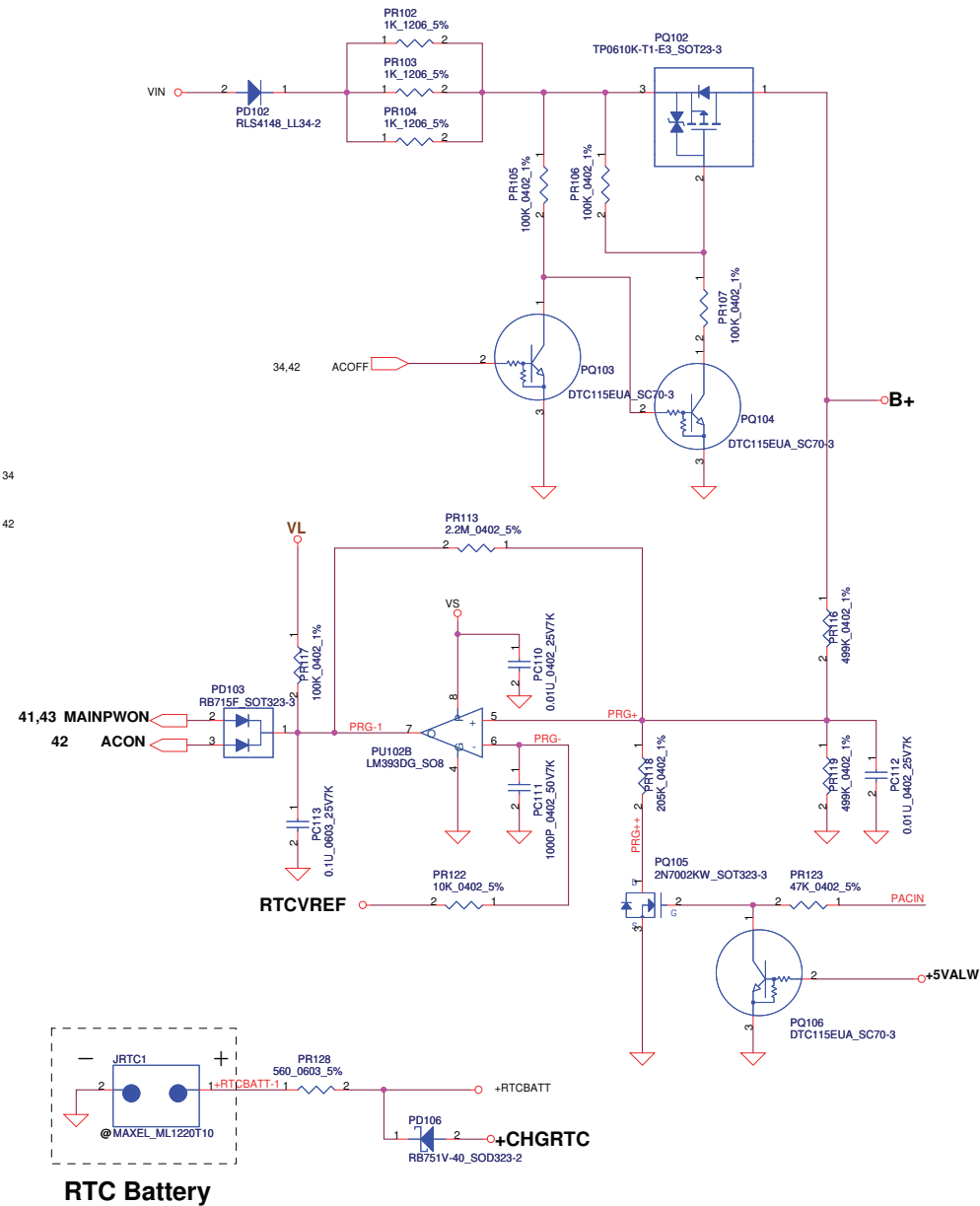
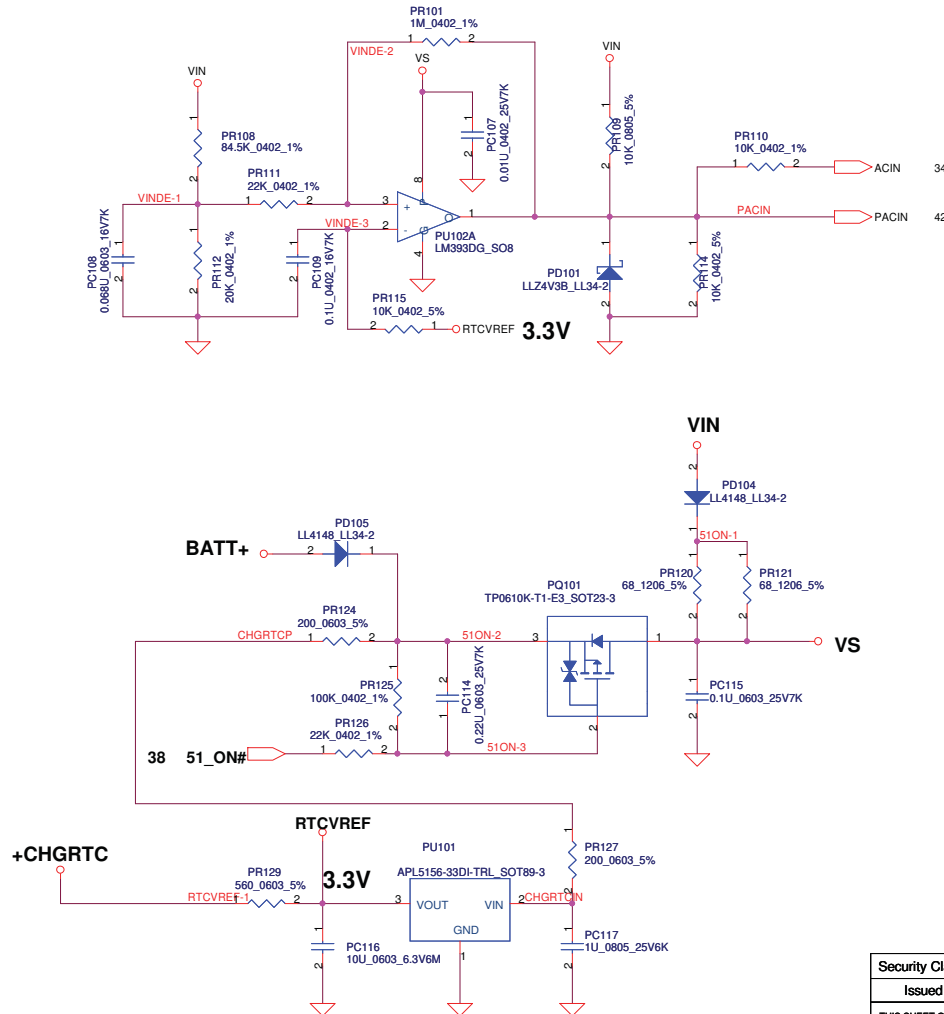
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Issued Date		Deciphered Date		Title	
2010/01/13		2011/01/13		DC Interface	
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Precharge detector		
	Min.	typ.
L-->H	14.991V	15.381V
H-->L	13.860V	14.247V

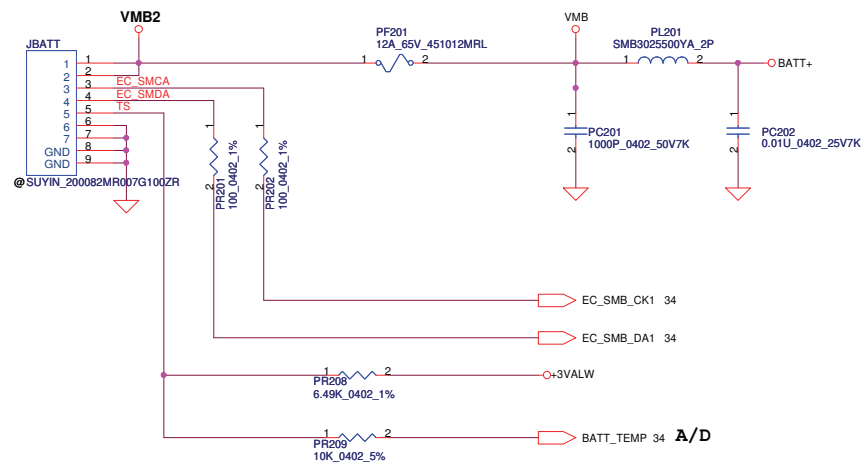
Precharge detector		
	Min.	typ.
L-->H	7.196V	7.349V
H-->L	6.138V	6.214V



Vin Detector		
	Min.	typ.
L-->H	17.430V	17.901V
H-->L	16.976V	17.262V



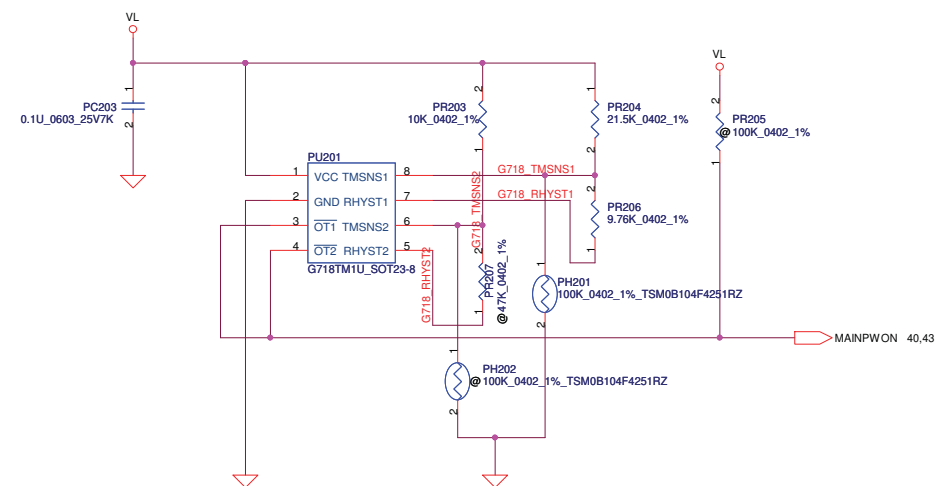
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	Custom	Rev	0.3	
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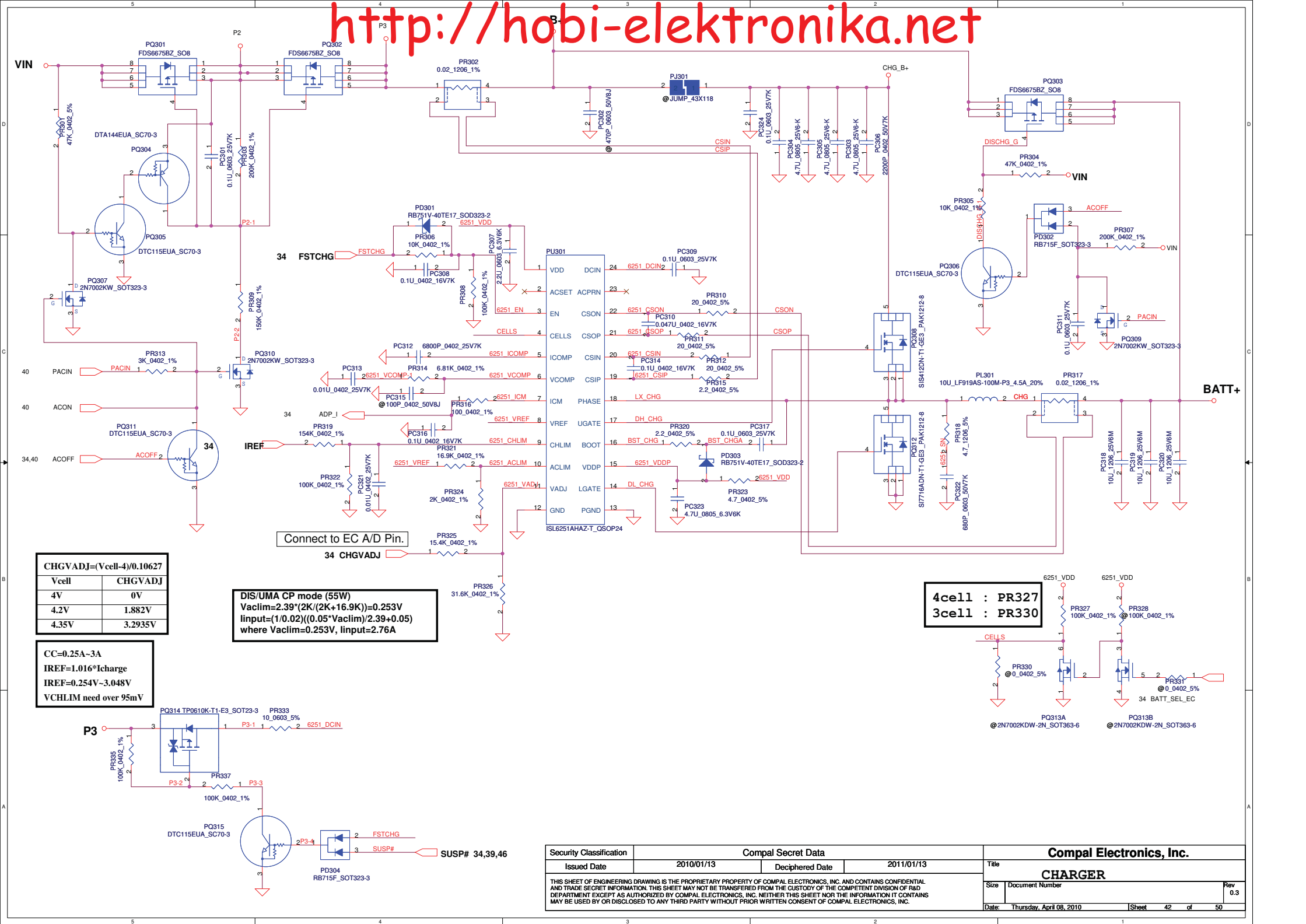


## PH1 under CPU botten side :

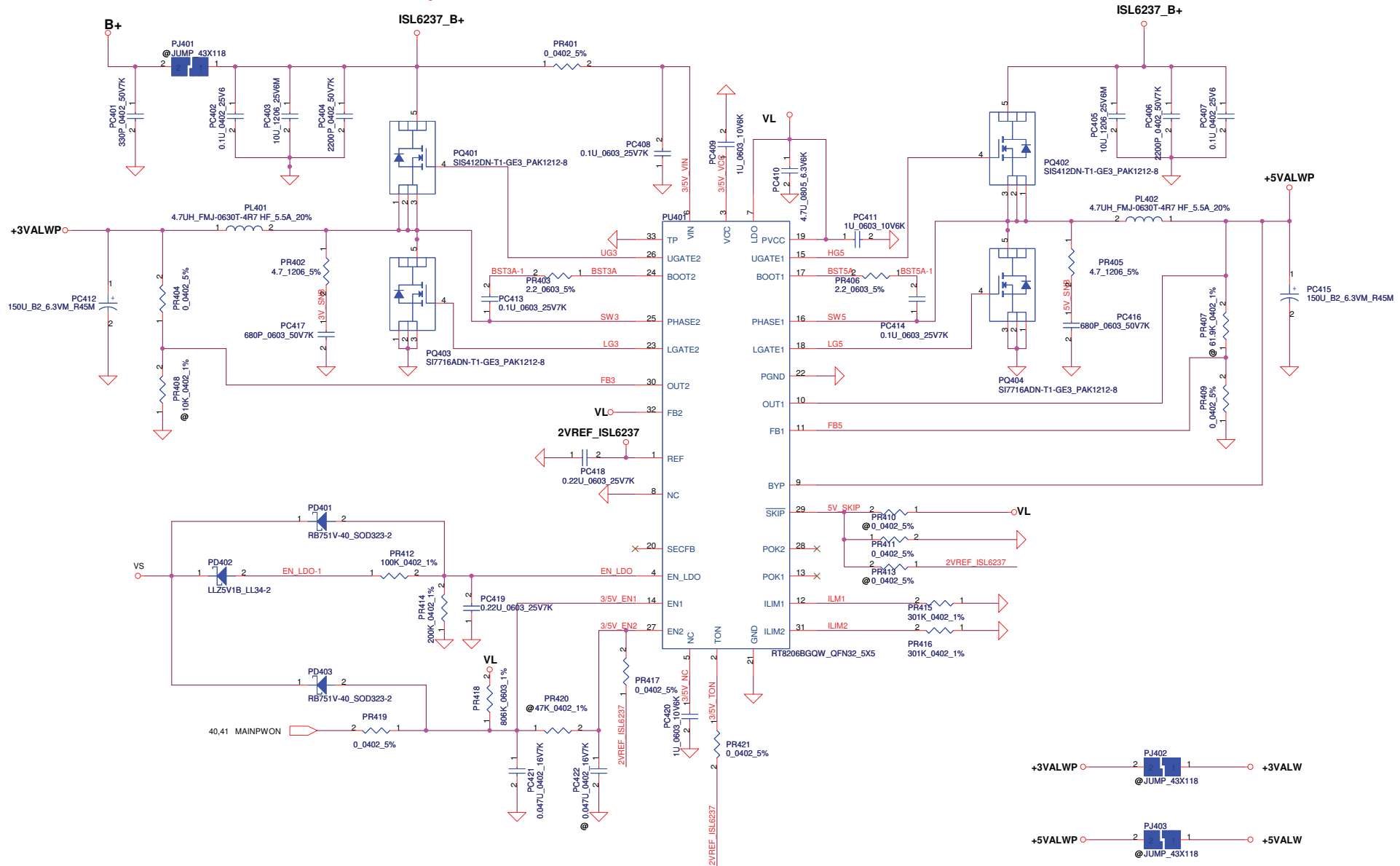
CPU thermal protection at 92 degree C

Recovery at 56 degree C

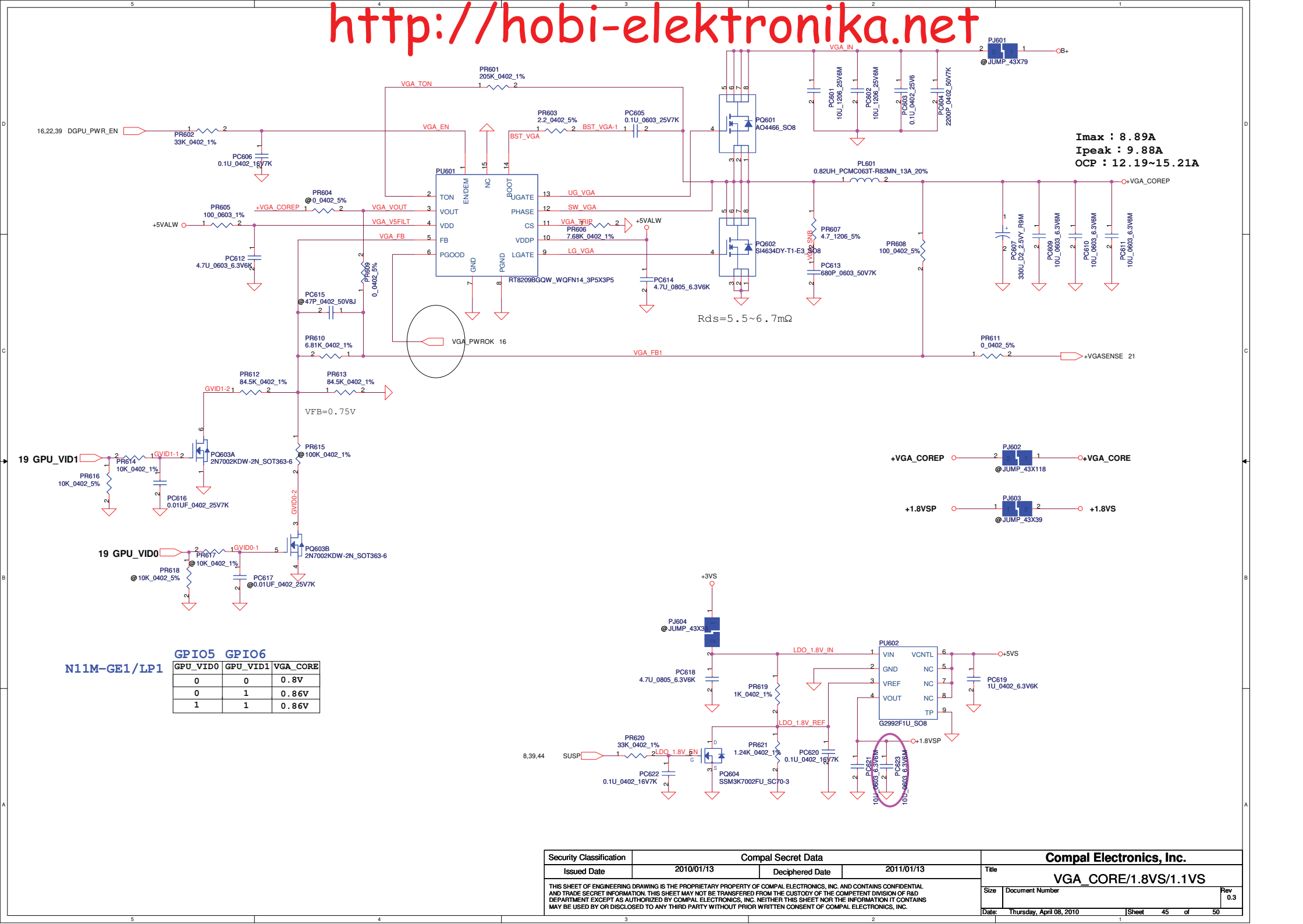


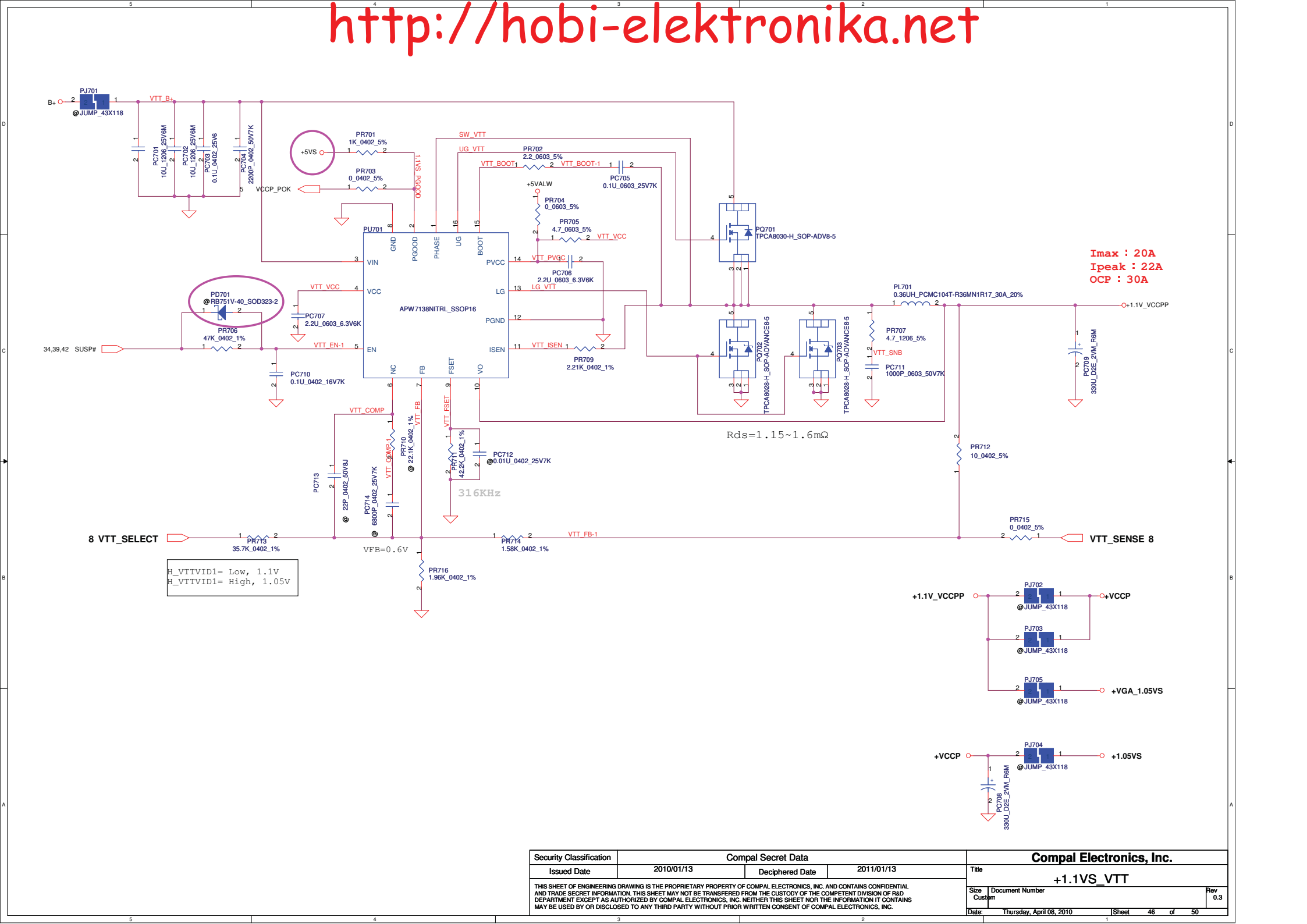












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**Compal Electronics, Inc.**

**Title**

**+1.1VS\_VTT**

**Size**

**Document Number**

**Rev**

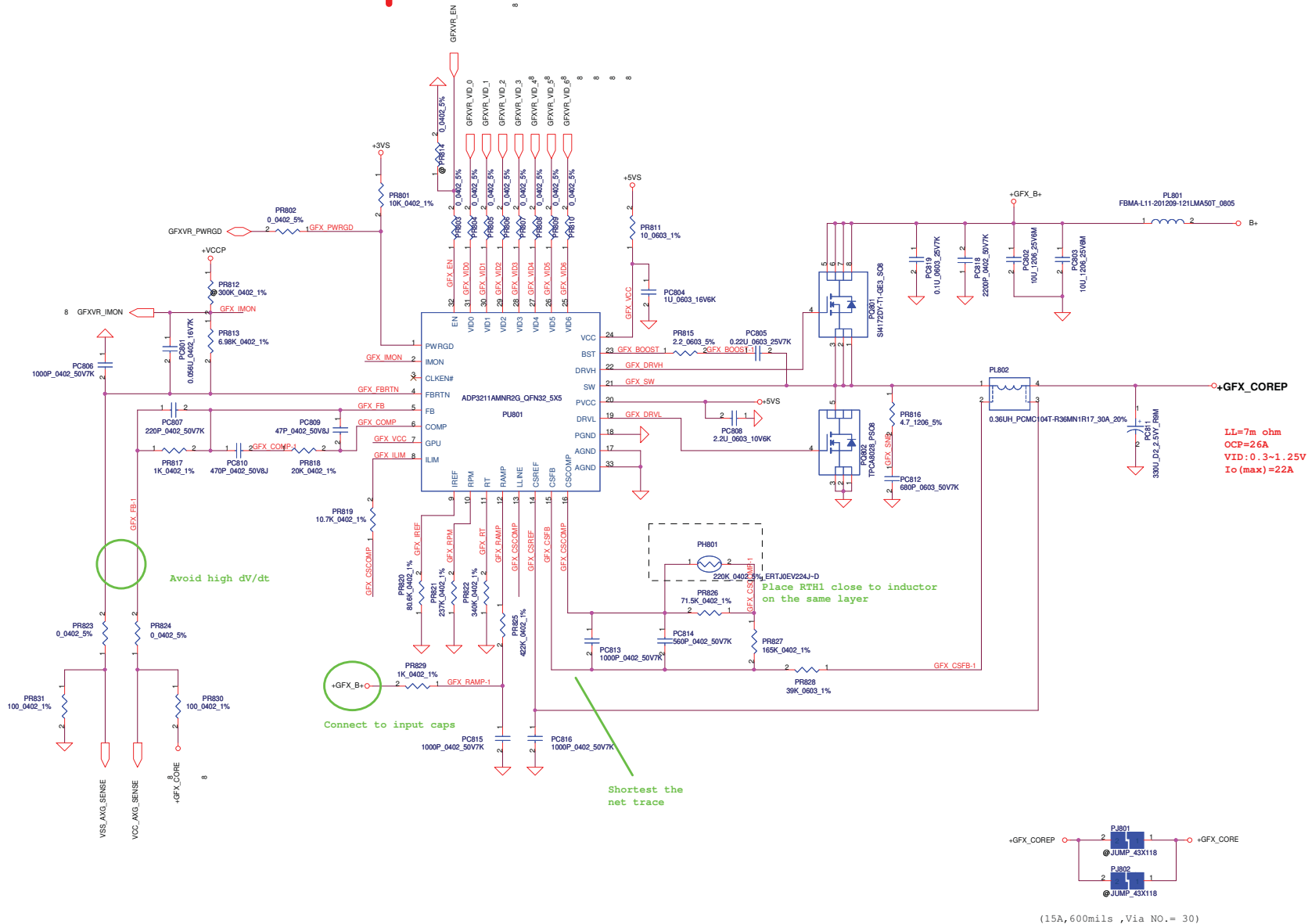
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**Date**

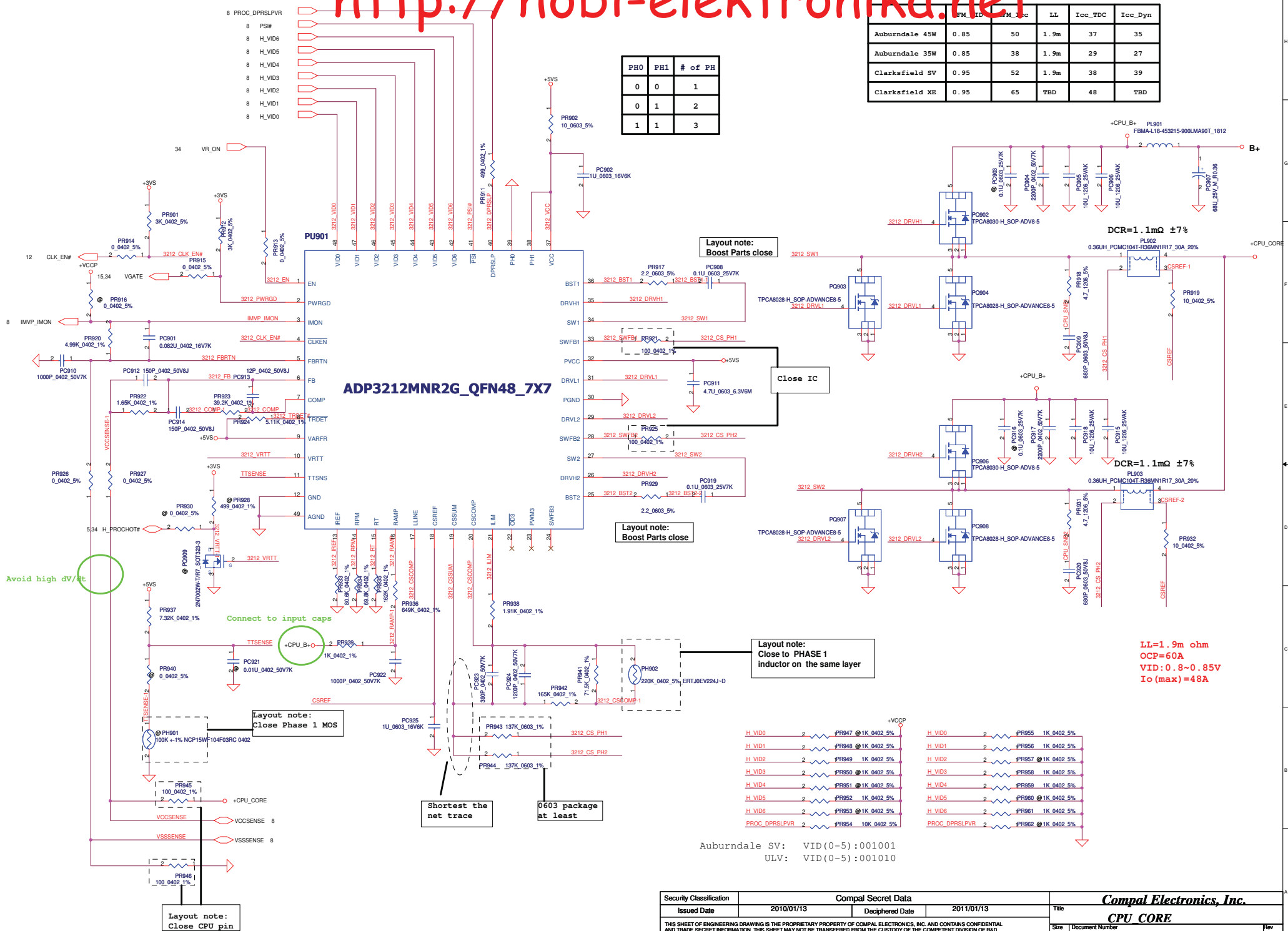
Thursday, April 08, 2010

**Sheet**

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PH0	PH1	# of P
0	0	1
0	1	2
1	1	3





Item	Reason for change	PG#	Modify List	Date	Phase
1	Add S3_0.75V_EN for 0.75 enable singal	44	Add PR523 and reserve PR521	11/09	Before A
2	Modify VGA GPIO table for NVIDIA SPEC.	45	Reserve PR615, PR617, PR618 and PC617 PR612, PR613 change to 84.5K from 100K	11/09	Before A
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

NO DATE PAGE			MODIFICATION LIST		PURPOSE	
-----						
1	30		RJ45 CONNECTOR		VER. R0_1030	
2	35		KB Matrix change			
3	31		EMC1403-1 change to EMC1403-2			
4	40, 42		POWER modify PQ313, PU102			
5			change USB port	FP : port10		
6			change USB power	USB3 : port 9		
7						
1102D MODIFY						
8	33		Add RA7, CA13	FOR ESD		
9	35		Add D22			
10	38		JFIR CONN. CHANGE TO 12 PIN			
11	36		CHANGE NET NAME			
12	27		JLVDS1 CONN. PIN SWAP.			
13	13		DEL CLRP1			
1104DMODIFY						
15	16		Add U15, R173, R177, R178, R627, R628			
1105DMODIFY						
17	28		Add Q44, Q45, Q49, Q55, Q60, Q62, R336			
18	26		Add Q61, Q63			
19	29		R726 change to 0805			
20	25		Add R559			
21	15		Add R180			
22	14		Add T24 PAD, T25 PAD			
23	8		Add R282			
24	14		Add R327, R325, T21 PAD			
1109DMODIFY						
25	14		Del R81, R83			
26	16		Add T26 PAD, C687			
27	27		Add R371, R372			
28	34		Del Q26, R303 T21PAD			
29	26		Add R230, Q17			
	5		Del Q61, Q63 Add Q99A, Q99B			
			Add Q61, R416			
		34		JFIR CONN change JLED CONN		
			add TP29, R320, R328, R230			
-----						
NO DATE PAGE			MODIFICATION LIST		PURPOSE	
-----						
1	MP	15	Add R687, R688		Intel DG	
2	MP	39	Add R5, Del R4		S5 power lost	

3

2

NO

DATE

PAGE

MODIFICATION LIST

PURPOSE

1

PVT

24

HDMI connector change to DIP type

DFB request

2

PVT

28

R336 change to 100Kohm

BOM error

3

PVT

38

D13,D14 change to panjit

cost down

4

PVT

38

RG4,RG5 chagne 56k ohm

RC filter for G-sensor output, EC request.

5

PVT

37

JBT1 change to 6 pin

For 6 pin BT module

6

PVT

34

SUSCLK connect to clock out

EC issued change note.

7

PVT

34

R978 45 to 0 ohm

For ECROM can't flash

8

PVT

34

Add Q63 2N7002, R344 10K

USB Power pulse when AC in, bug

9

PVT

34

Add net CLKRUN# on pin38

reserve for power saving

10

PVT

34

32.768KHz change to 70x15x1.4

cost down

11

PVT

13

32.768KHz change to 70x15x1.4

cost down

12

PVT

33

INT\_MIC\_CLK add CA18 100pF cap.

EMI request

13

PVT

33

Audio pin4 add D7

Realtek change note for bug

14

PVT

28

Add Q45 2N7002

For Wimax LED no function, bug

15

PVT

27

change U42 to ST

cost down

16

PVT

27

Add Q64,Q37,R440

cost down, enable bkl circuit

17

PVT

26

Add R322,R328 0 ohm

For "non-PnP device" bug

18

PVT

22

Add R474 34.8K ohm

N-vidia N11M-LP1 device ID

19

PVT

19

L7,L8,L17,L18 change to 0 ohm

for EDID can't detect sometime, cost down

20

PVT

17

R208 change to 1 ohm

CRT garbege in uma mode

21

PVT

16

R580 add 0 ohm

for bug, uma switch to dis will hang up

22

PVT

15

R175 2.2k to 4.7k ohm

common design update

23

PVT

12

Y1 14.318MHz change to 5032 size

common design

24

PVT

09

C75,C76,C92,C164 change to 333uF 6m ohm

cost down

25

PVT

X

Q4,QG1,Q32,Q33,Q73,Q74,Q75,Q97 change to A03413

cost down

26

PVT

34

Add R345 10Kohm

EC\_TACH pull up

NO

DATE

PAGE

MODIFICATION LIST

PURPOSE

1

SVT

39

Add R568, Q40

+0.75VS discharge

2

SVT

39

Add R673 10K

+1.5V EN pin pull down

3

SVT

39

Change U33 to Low Rds-on type

VRAM voltage drop

4

SVT

37

Add EMI common chock on USB pl,p0;L38,L39

EMI

5

SVT

34

CLKRUN# pull down, R671 10K

common design

6

SVT

34

Reserve R685 for WLAN\_LED by EC control

WLAN LED

7

SVT

33

ALC259 change to VB

Version change

8

SVT

29

del R654 leakage

leakage

9

SVT

28

WLAN LED control change to DTL AND gate

For some card design

10

SVT

27

Add U6,U17,U18,U19 for BKL and PWM control

signal select switch

11

SVT

27

Add R370 680ohm

support No color engine panel

12

SVT

27

Add D36

LCEVDD discharge

13

SVT

26

Reserve CRT double pi filter

Vidio Filter

14

SVT

25

Add R670 2.2K

HDMI common design

15

SVT

15, 25

Add R675,R674 100K

Hybrid mode disable PCH HDMI

16

SVT

17

C505,C492 change size 0603

ME demend

17

SVT

17

C447 change to 1uF

common design

18

SVT

13

Add R677

HDA SDIN1

19

SVT

8

Change R268 to 47K

timing

20

SVT

8

Add R551 1K

PSI# pull down, strip pin

21

SVT

5

C338 change to 0.047uF

common design, S3 shutdown

22

SVT

5

R135 remove

warm boot issue

23

SVT

12

Add C365

10pF for RF

24

SVT

14

Add R413,C439 22ohm,10pF

For RF

File